Heterojunction oxide thin-film transistors with unprecedented electron mobility grown from solution

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Thin-film transistors made of solution-processed metal oxide semiconductors hold great promise for application in the emerging sector of large-area electronics. However, further advancement of the technology is hindered by limitations associated with the extrinsic electron transport properties of the often defect-prone oxides. We overcome this limitation by replacing the single-layer semiconductor channel with a low-dimensional, solution-grown In2O3/ZnO heterojunction. We find that In2O3/ZnO transistors exhibit band-like electron transport, with mobility values significantly higher than single-layer In2O3 and ZnO devices by a factor of 2 to 100. This marked improvement is shown to originate from the presence of free electrons confined on the plane of the atomically sharp heterointerface induced by the large conduction band offset between In2O3 and ZnO. Our finding underscores engineering of solution-grown metal oxide heterointerfaces as an alternative strategy to thin-film transistor development and has the potential for widespread technological applications.

INTRODUCTION

Transparent metal oxides have emerged as a promising family of compound semiconductors for a range of applications in the field of large-area optoelectronics because of a variety of assets, including tunable energy band structure, high charge carrier mobility, optical transparency, mechanical flexibility and durability, and outstanding chemical stability (1–5). A further prominent asset is their ease of processing from solution phase at low temperatures (6, 7) and under ambient conditions that would alter our perception and modus operandi in semiconductor industry by gradually abolishing established vacuum-based process technologies for widespread technological applications, especially in the field of thin-film transistor (TFT) electronics. Currently, metal oxide TFTs with electron mobilities exceeding 10 cm2/V·s have been achieved (8–13), and numerous new approaches to further enhance the device performance have been proposed and demonstrated (6, 14, 15). It is now well established that the measured carrier mobility may be affected by several factors, including (i) the intrinsic mobility of the semiconductor used, (ii) the microstructural quality of the semiconducting layer, and (iii) the device architecture itself.

A notable strategy that has been successfully used to enhance the performance of metal oxide TFTs in the past few years is based on the use of multilayer channels (16–21). Although the exact mechanism(s) underpinning performance enhancement is still under debate, it has been proposed that under certain circumstances, electron transfer and confinement at the heterointerface can occur because of conduction band (CB) offset (17, 21–23) in a process similar to that observed in conventional high electron mobility transistors (HEMTs) made of AlGaAs/GaAs heterointerface channels (24–29). In these devices, the formation of a two-dimensional electron gas (2DEG) at the critical heterointerface enables the realization of transistors with electron mobilities close to the theoretical limit set by phonon scattering in the semiconductor (27–29). In terms of the underlying transport physics, metal oxide–based TFTs that resemble traditional HEMTs have been produced by various growth techniques, including radio-frequency (RF) sputtering (16, 30), molecular beam epitaxy (MBE) (31), metalorganic chemical vapor deposition (MOCVD) (32), and atomic layer deposition (21).

One of the most extensively studied metal oxide heterointerface systems that is known to lead to 2DEG formation is that of ZnO/ZnMgO (33–37). The latter relies on electron confinement at the heterointerface due to a large CB offset and polar surfaces (34, 35). For optimal interface quality, epitaxial material growth is commonly carried out via MBE or pulsed laser deposition on single-crystal substrates, such as sapphire or ScAlMgO4 (33, 37). However, it was shown that 2DEG could also form in ZnO/ZnMgO heterointerfaces grown on glass substrates via less elaborate techniques, such as RF sputtering (36). Despite their polycrystalline nature, the heterointerfaces exhibited enhanced sheet electron concentration and mobility with a characteristic temperature-independent behavior (36).

We recently reported evidence of quantized energy states in low-dimensional, solution-grown In2O3 (38) and ZnO layers (39) and demonstrated metal oxide superlattice TFTs with electron mobilities in the range of 25 to 45 cm2/V·s (22). However, these archetype devices rely on complex manufacturing and involve elaborate multilayered architectures (21, 22). Thus, a major challenge in further advancing the performance of metal oxide TFTs lies in the development of high-quality oxide heterostructures via scalable manufacturing processes (7).

Here, we report the growth of low-dimensional metal oxide heterostructures consisting exclusively of In2O3 and ZnO layers grown from solution phase and their implementation in high electron mobility TFTs. We show that ultrathin (<13-nm) In2O3/ZnO heterojunctions can be grown reliably over large areas at 25°C in a process of ultrasonic spray pyrolysis and spin coating. Remarkably, charge transport in In2O3/ZnO heterojunction transistors is found to be consistently superior to single-layer devices with maximum electron mobility values in excess of 45 cm2/V·s. The high electron mobility is accompanied by a marked change in the charge transport mechanism, both of which are attributed to the synergistic effects of the atomically sharp In2O3/ZnO...
RESULTS

We fabricated bottom-gate, top-contact transistors based on solution-grown ZnO, In$_2$O$_3$, and In$_2$O$_3$/ZnO heterostructures using aluminum (Al) source-drain (S-D) electrodes. Epitaxial-like 4- to 7-nm-thick In$_2$O$_3$ layers were grown by ultrasonic spray pyrolysis (Fig. 1A) in air at 250°C (8), whereas 4- to 6-nm-thick polycrystalline layers of ZnO were processed via spin coating and thermal annealing at 210°C (Fig. 1B) (39). In$_2$O$_3$/ZnO heterostructures were fabricated via sequential deposition of In$_2$O$_3$ by ultrasonic spray pyrolysis and spin casting of ZnO at 250° and 210°C, respectively. TFT fabrication was completed with the deposition of the top Al S-D electrodes via vacuum sublimation (Fig. 1C).

Figure 1D shows the transfer characteristics (drain current $I_D$ versus gate voltage $V_G$) of single-layer In$_2$O$_3$ and ZnO TFTs, as well as of an In$_2$O$_3$/ZnO heterojunction device. First, we consider the characteristics of In$_2$O$_3$ and ZnO transistors to benchmark the level of performance of the single-layer semiconductor devices. All In$_2$O$_3$ transistors exhibit a typical n-channel behavior with electron field-effect mobility ($\mu_{FE}$) of ~16 cm$^2$/V·s and channel current on/off ratios of 10$^6$, in accordance with previous work (8). On the other hand, ZnO transistors processed via spin coating exhibit high turn-on voltages $V_{ON}$ (~40 V) and a relatively low $\mu_{FE}$ of <1 cm$^2$/V·s. Although the In$_2$O$_3$/ZnO heterojunction transistor exhibits a channel current on/off ratio and $V_{ON}$ similar to the In$_2$O$_3$ device, it can sustain significantly higher currents, most likely due to the increased electron channel mobility. Analysis of the transfer characteristics in Fig. 1D reveals that In$_2$O$_3$/ZnO transistors exhibit nearly 100× higher $\mu_{FE}$ than ZnO devices and at least a factor of 2 higher than In$_2$O$_3$ transistors with average and peak $\mu_{FE}$ of ~30 and ~45 cm$^2$/V·s, respectively. The impact of $\mu_{FE}$ on the current driving capabilities of the TFTs is better illustrated in Fig. 1E, where the output characteristics of In$_2$O$_3$ and In$_2$O$_3$/ZnO transistors are shown. The threshold voltage $V_T$ of the heterojunction transistors is also found to be consistently more negative (~7.3 V) when compared to In$_2$O$_3$ TFTs (~1.3 V) (Fig. 1F), suggesting the existence of a higher electron concentration in the channel, the origin of which will be discussed below. Evidently, the In$_2$O$_3$/ZnO heterojunction TFT can sustain significantly larger currents than the In$_2$O$_3$ device, which is a direct consequence of the greatly enhanced electron mobility.

To elucidate the origin of the stark difference in electron transport measured between In$_2$O$_3$, ZnO, and In$_2$O$_3$/ZnO transistors, we analyzed the gate-voltage dependence of $\mu_{FE}$ according to the power law equation (30)

$$\mu_{FE} = K (V_G - V_{TP})^\gamma$$

where $V_G$, $V_T$, and $V_{TP}$ are the gate, percolation, and threshold voltages, respectively, whereas the prefactor K and the exponent $\gamma$ relate to the nature of the transport mechanism. Specifically, the prefactor K includes the percolation term from the Thomas-Fermi approximation (40) for both trap-limited conduction (TLC) and percolation conduction (PC). For the latter case, $\mu_{FE}$ also includes the contribution of the spatial characteristics of the potential barriers. On the other hand, the power exponent $\gamma$ depends either on the temperature $T$ for TLC or the spatial characteristics of the potential barriers for PC. Consequently, its value is indicative of the different charge transport processes that dominate channel conduction. Lee et al. (30) have recently shown that a $\gamma$ value close to 0.7 indicates TLC, whereas a value of ~0.1 indicates a PC-dominated process. As shown in Fig. 1G and fig. S1, the $\mu_{FE}$ evolution for the In$_2$O$_3$ device can be fitted over a wide range of $V_{GS}$ values using $\gamma = 0.66$, indicating TLC as the dominant conduction process. On the other hand, for In$_2$O$_3$/ZnO heterojunction TFTs, $\gamma$ varies from 0.7 to 0.11 for lower and higher gate fields, respectively, suggesting a transition from a TLC-dominated to a PC-dominated process.

Further experimental evidence on the existence of starkly different electron transport mechanisms between the two types of devices is provided by the temperature dependence of $\mu_{FE}$ evaluated in the linear bias regime $\mu_{LIN}$. Figure 1H displays the Arrhenius plots of $\mu_{LIN}$ between 78 and 300 K for In$_2$O$_3$ and In$_2$O$_3$/ZnO transistors. Evidently, the In$_2$O$_3$ device exhibits a temperature-activated behavior, which is a typical characteristic of TLC, where $\mu_{LIN}$ remains constant (3 to 4 cm$^2$/V·s) in the temperature range of 78 K $\leq T \leq$ 160 K, followed by an exponential increase for $T >$160 K to a maximum value of ~12 cm$^2$/V·s at room temperature. The activation energy $E_A$ determined from the 160 K $\leq T \leq$ 300 K region is ~40 meV and is associated with the presence of electron traps in the In$_2$O$_3$ layer. A similar behavior is observed for single-layer ZnO TFTs and is consistent with TLC because the $\gamma$ exponent of $\mu_{LIN}$ does depend on the temperature (30). In contrast, In$_2$O$_3$/ZnO heterojunction devices exhibit a temperature-independent $\mu_{LIN}$ across the entire temperature range investigated (78 to 300 K). These results indicate that electron transport in In$_2$O$_3$/ZnO TFTs is most likely governed by PC, which is exclusively associated with the spatial distribution of the potential barriers (30). Therefore, the electrical measurements point to the fact that the electron conduction process in single-layer In$_2$O$_3$ and ZnO TFTs is fundamentally different from that in In$_2$O$_3$/ZnO heterojunction devices.

To determine the origin of the different electron transport mechanisms, we investigated the surface topography of each oxide layer by means of intermittent contact mode atomic force microscopy (AFM). Figure 2 (A to D) shows AFM images for Si$^+/+$SiO$_2$, Si$^+/+$SiO$_2$/In$_2$O$_3$, Si$^+/+$SiO$_2$/ZnO, and Si$^+/+$SiO$_2$/In$_2$O$_3$/ZnO. The differences between the various surface topographies are better illustrated in the height histograms of Fig. 2E. As expected, SiO$_2$ exhibits a featureless and atomically smooth topography with a root mean square (RMS) roughness ($\sigma_{RMS}$) of ~0.18 nm. Remarkably, spray-grown In$_2$O$_3$ layers (Fig. 2B) also exhibit very flat surfaces with $\sigma_{RMS} = 0.42$ nm. We note that the latter value is less than half of the unit cell size of cubic In$_2$O$_3$ (41), and as a result, the sample’s surface appears almost featureless over several micrometers. The latter is comparable to the surface characteristics of semiconductor quantum-well structures grown via sophisticated vacuum-based techniques, such as MBE (42), MOCVD (43), and metalorganic vapor phase epitaxy (44), despite being processed by ultrasonic spray pyrolysis in ambient atmosphere. Contrary to In$_2$O$_3$, the surface topography of single-layer ZnO (Fig. 2C) reveals the existence of crystallites with a relatively high surface roughness of $\sigma_{RMS} \sim 1.57$ nm. When ZnO is spin-coated onto In$_2$O$_3$ to form the In$_2$O$_3$/ZnO heterojunction (Fig. 2D), a similar surface topography is observed but with the ZnO crystallites appearing slightly enlarged. We attribute this to the different contact angles of aqueous solutions on SiO$_2$ and In$_2$O$_3$ surfaces and the different conditions under which ZnO crystallization and growth occur (45, 46). These larger ZnO crystallites are responsible for the increased surface roughness ($\sigma_{RMS} = 2.32$ nm) of the In$_2$O$_3$/ZnO heterojunction (Fig. 2E).
The microstructure of the In$_2$O$_3$/ZnO heterojunctions was further examined by high-resolution transmission electron microscopy (HRTEM). Figure 3A shows the cross-sectional HRTEM image of a representative In$_2$O$_3$/ZnO heterojunction grown on SiO$_2$. The thickness of this particular heterojunction is approximately 10 nm and is characterized by the atomically sharp In$_2$O$_3$/ZnO heterointerface—a truly remarkable finding if one considers the simplicity of the solution deposition techniques used. For this particular sample, the ZnO layer was 4–7 nm thick and featured randomly oriented nano-crystals on the surface of In$_2$O$_3$. On the contrary, the In$_2$O$_3$ layer had the form of highly crystalline elongated platelets that are 4 to 5 nm thick. Geometric phase analysis (GPA) performed with a spatial resolution of 0.4 nm confirms that the microstructure of In$_2$O$_3$ is that of elongated platelets with an average length of 35 ± 5 nm along the lateral direction (see section S2). Although no persistent growth texture for the In$_2$O$_3$ crystals could be identified, there is a trend amid them to grow with the [001] direction of their Ia$\overline{3}$m body-centered cubic (bcc) crystal lattice roughly parallel (fig. S2), or occasionally perpendicular, to the SiO$_2$.
surface. Fast Fourier transform (FFT) analysis (Fig. 3B) of the highlighted regions in Fig. 3A provided further evidence that the ZnO layer is nanocrystalline with the three prominent spacings corresponding to the [202], [110], and [101] planes of the hexagonal wurtzite structure, whereas for the In2O3 layer, the lattice spacing of 0.36 nm corresponds to the [220] crystal plane of the bcc structure of In2O3. Although no straightforward structural relation between the In2O3 and ZnO layers could be identified, the heterointerface is continuous with no evidence of materials intermixing (Fig. 3A and fig. S3). This interesting microstructural feature may be due to the chemistry and low viscosity of the ammonium hydroxide–based precursor formulation used to grow the ZnO layers. Thus, the HRTEM data verify that sequential solution deposition of In2O3 and ZnO leads to the formation of a seamless In2O3/ZnO heterojunction with low interface roughness and without evidence of alloying (see section S2).

We have combined x-ray photoelectron spectroscopy (XPS) with mild in situ Ar+ etching (Fig. 4A) to study the electronic states in bare In2O3 and In2O3/ZnO heterojunction as a function of etching depth. The same method was also used to acquire the elemental profile and energy band structure of the In2O3/ZnO heterointerface. The integral area of the In-3d, Zn-2p, O-1s, C-1s (adventitious carbon), and Si-2p photoelectron lines was used after background subtraction and taking
into account the relevant sensitivity factors. ZnO exhibit a slight oxygen deficiency, whereas In$_2$O$_3$ is nearly stoichiometric. For the chemical analysis of the layers, special attention was given to the O-1s core-level spectra (fig. S4), which are very sensitive to the chemical state of O and to the neighboring atoms (8, 47–49). Ultrathin layers of ZnO and In$_2$O$_3$ were found to contain Zn–O and In–O bonds in their respective lattice sites, with minor contributions from Zn–OH and In–OH detected on their surfaces.

Figure 4B shows the depth-resolved elemental composition of the low-dimensional In$_2$O$_3$/ZnO heterostructure acquired through successive XPS spectra at varying etching time (depth). The small amount of In detected at the surface of the heterojunction (etching time, 0 s) is attributed to the small layer thickness of ZnO (4 to 6 nm), which is comparable to the escape depth of the In-3d photoelectrons. The same applies for the In$_2$O$_3$ layer because it is transparent to the Si-2p photoelectrons, resulting in the apparent presence of Si at an etching time of ~150 s. The XPS data are in agreement with HRTEM analysis (Fig. 3) and verify the structural and chemical composition of the In$_2$O$_3$/ZnO heterojunction.

Figure 4C shows the In-3d core-level spectra recorded at different etching times for bare In$_2$O$_3$ (dashed lines) and In$_2$O$_3$/ZnO heterojunction (solid lines) (more details on the In-3d and Zn-2p core-level spectra are presented in figs. S5 to S8 and in the relevant discussion found in the online Supplementary Materials). No spectral variation in the core-level spectra of bare In$_2$O$_3$ is observed (dashed lines), with increasing etching time indicating a size-independent electronic structure. On the contrary, there is a strong dependence of the In-3d core-level spectra with etching depth for the SiO$_2$/In$_2$O$_3$/ZnO heterojunction (solid lines). The latter is attributed to the Fermi level pinning due to electron transfer from ZnO to In$_2$O$_3$ (22). To quantify this effect, we studied the valence band offset (VBO) between ZnO and In$_2$O$_3$ using the experimentally determined relative spectral positions of the Zn-2p and In-3d core levels, taking into account the value of the upper edge of the VB spectra of bulk In$_2$O$_3$ and ZnO (fig. S9) and following the method proposed by Kraut et al. (50). The VBO between the In$_2$O$_3$ and ZnO can be determined using the equation

$$VBO = (E_{In-3d}^{bulk} - E_{In-VB}^{bulk}) - (E_{Zn-2p}^{bulk} - E_{Zn-VB}^{bulk}) - (E_{In-3d}^{exp} - E_{Zn-2p}^{exp})$$


Fig. 4. XPS analysis of single-layer In$_2$O$_3$ and In$_2$O$_3$/ZnO heterojunctions. (A) Schematic drawing of the XPS depth profiling measurement setup. (B) Elemental depth profile of the bilayer film stack on the Si/SiO$_2$ substrate. Inset: HRTEM image of the heterointerface studied by XPS where the vertical dashed lines indicate the In$_2$O$_3$/ZnO interfaces. (C) The evolution of the spectral position of the In-3d core level with respect to the etching time for SiO$_2$/In$_2$O$_3$/ZnO (solid lines) and for SiO$_2$/In$_2$O$_3$ (dashed lines); note that the times indicated for the SiO$_2$/In$_2$O$_3$/ZnO system correspond exclusively to ZnO etching. (D) The VBO between ZnO and In$_2$O$_3$ versus the thickness of the ZnO overlayer determined from Eq. 2. (E) Energy band diagram of the In$_2$O$_3$/ZnO heterointerface reconstructed on the basis of XPS, optical absorption, and Kelvin probe measurements. Energies are shown with respect to (w.r.t.) Fermi energy, $E_F$, and vacuum level.
where In-3d and Zn-2p are the spectral positions of the corresponding core-level spectra, and VB indicates the upper edge of the VB spectra of bulk In₂O₃ and ZnO. “bulk” and “exp” superscripts indicate the values obtained from bulk (>20 nm) and ultrathin films (<10 nm), respectively. Figure 4D shows the evolution of the VBO between In₂O₃ and ZnO for varying ZnO thickness, which was determined by monitoring the Zn-2p and In-3d core levels after each etching step. VBO reaches a constant value of ~1 eV for a ZnO thickness of ~5 nm. The corresponding CB offset can be determined by considering the bandgap energy E_g of the individual In₂O₃ (3.76 eV) and ZnO (3.33 eV) layers (see fig. S10). Figure 4E shows a schematic of the resulting energy band diagram of the In₂O₃/ZnO heterojunction. The electron transfer from the CB of ZnO to that of In₂O₃ is attributed to the CB offset, resulting in the formation of a spatially confined sheet of free electrons at the vicinity of the interface on the In₂O₃ side. To verify the existence of the confined charge, we evaluated the electron concentration across the heterojunction using capacitance-voltage (C-V) analysis of metal-insulator-semiconductor capacitor structures. The C-V technique is often used to verify the presence and location of the confined charges across the heterostructures because it enables quantitative analysis of the apparent free carrier concentration with high spatial resolution (33, 34). In heterointerfaces where a 2D-confined sheet of electrons is present, a clear spike in the carrier profile should exist, indicating the exact position of the critical interface (33, 34). The experimental results shown in fig. S11 (A and B) reveal the presence of an increased concentration of free electrons located right at the expected position of the In₂O₃/ZnO heterointerface. The spike in the electron profile reaches a maximum value of ~3.1 × 10¹⁹ cm⁻³ and has a width of 1 to 2 nm. The latter value is expected to be determined primarily by the interface roughness and is in agreement with the surface height histograms in Fig. 2E. The CB discontinuity evaluated via XPS and optical absorption spectroscopy measurements, combined with the high structural quality of the In₂O₃/ZnO heterointerface and the presence of a 2D-confined sheet of electrons at the heterointerface, supports the PC mechanism observed in In₂O₃/ZnO transistors.

**DISCUSSION**

For the first time, low-dimensional and atomically sharp In₂O₃/ZnO heterojunctions have been grown from solution phase at low temperatures and incorporated in TFTs. Although heterojunction oxide TFTs have been previously realized using various solution-processed amorphous ternary and quaternary metal oxide compounds, such as InZnO, AlInZnO, or InGaO (19, 20, 51–53), it has been proven challenging to increase the electron mobility beyond values obtained from the individual constituent materials (23). The In₂O₃/ZnO heterojunction transistors developed in this work not only surpass the performance of single-layer In₂O₃ and ZnO TFTs but also compare favorably to state-of-the-art vacuum-processed devices (4, 9, 54). The exceptional level of performance is attributed to three main factors: (i) the ability to grow highly crystalline In₂O₃ layers via ambient ultrasonic spray pyrolysis (Fig. 3), (ii) the formation of a seamless and dislocation-free In₂O₃/ZnO heterointerface upon sequential deposition of the top ZnO layer via spin casting (Fig. 3A), and (iii) the existence of a sheet of free electrons confined in the x-y plane of the atomically sharp In₂O₃/ZnO heterointerface due to the large CB discontinuity (Fig. 4E). Additional factors that could potentially contribute to the enhanced performance include the passivation of In₂O₃ surface defects by ZnO and/or the suppression of the injection barrier for electrons due to Schottky barrier lowering because of the existence of surface electron accumulation.

The combined effects of these unique attributes results to the marked change in the electron transport mechanism manifested first as an increase in electron mobility (Fig. 1D) and, second, in the transition from a trap-limited to a percolation-dominated conduction process (Fig. 1G). Further evidence supporting this fundamental change is provided by the temperature dependence of 1/τ_In, where the temperature-activated electron transport in single-layer In₂O₃ devices (Fig. 1H) transforms to a temperature-independent behavior for In₂O₃/ZnO heterojunction TFTs, which is a characteristic indicative of trap-free band-like electron transport not previously observed in metal oxide TFTs.

The presence of a smooth and highly crystalline In₂O₃ layer is of critical importance because it facilitates the formation of the atomically sharp In₂O₃/ZnO heterointerface upon sequential processing of the top ZnO layer without alloying (Fig. 3A). The latter feature combined with the significant CB energy offset between In₂O₃ and ZnO (Fig. 4E) results in the formation of a space charge layer that is confined in the out-of-plane z direction but highly delocalized along the 2D heterointerface. This quasi-2D free-electron system, which was experimentally determined for the first time by depth-resolved XPS (Fig. 4, C to E) and C-V carrier profiling measurements (fig. S11), facilitates a substantial increase in the concentration of free electrons within the crystalline In₂O₃ layer while avoiding adverse effects associated with Coulomb scattering that are often seen in conventional doped semiconductor transistors (17, 28). To this end, one may also argue that the higher electron concentration would shift the Fermi energy of the heterojunction closer the CB of In₂O₃ (Fig. 4E), facilitating access to the extended states which would otherwise have remained inaccessible. On the other hand, the ultrathin nature of the In₂O₃ layer (Fig. 3A) may lead to quantization of the energy states (subbands) (38) perpendicular to the transport plane (z direction) without affecting their in-plane delocalization. The low-dimensional and exceptional structural quality of these solution-grown In₂O₃ layers could one day lead to the observation of transport processes similar to those reported for traditional 2DEG heterojunction devices (18, 28). However, more work is required to reveal the true potential of these systems and devices based on them.

Although this work focuses on the In₂O₃/ZnO heterointerface, our findings provide guidelines for the design of metal oxide TFTs with performance characteristics potentially superior to any existing thin-film semiconductor technology, either via further heterointerface engineering or through the use of different materials and/or advanced doping schemes (27–29). For example, incorporation of suitable seed layers deposited from solution onto the substrate could assist in controlling and hence improving the crystal quality of the subsequently deposited In₂O₃ layer with direct impact on the quality of the resulting heterointerface. Similarly, n-type doping of ZnO using newly developed routes (55) could provide an additional parameter that could be exploited to tune the confined electrons, and hence the TFT characteristics, in a similar manner to modulation-doped AlGaAs/GaAs heterojunction field-effect transistors (27–29, 56). More broadly, the use of high-mobility In₂O₃/ZnO heterointerfaces could be extended to transparent conductive electrodes, where the incorporation of multiple “charged” high-mobility heterointerfaces could be exploited to increase the layer conductivity of solution-processed transparent superlattices, hence enabling their use as conductive electrodes in large-area optoelectronics.

Last, our results identify the use of solution-grown In₂O₃/ZnO heterointerfaces as a powerful method to enhance the electron transport
in metal oxide TFTs beyond single material–based devices. It also suggests that solution-processed, low-dimensional metal oxide semiconductors could well be entering the realm of quantum electronics and that the resulting devices may one day compete directly with mature semiconductor technologies but with the added advantage of being produced at a small fraction of the cost.

**MATERIALS AND METHODS**

**Precursor solutions and deposition techniques**

Metal oxide semiconductors were deposited in ambient air either via ultrasonic spray pyrolysis (In$_2$O$_3$) or spin coating (ZnO). For spray pyrolysis of In$_2$O$_3$, indium nitrate [\(\text{In(NO}_3\text{)}_3\)] (99.99%, Indium Corporation of America) was dissolved in deionized (DI) water at a concentration of 30 mg/ml. The resulting solution was stirred at room temperature for 30 min and subsequently sprayed onto the heated sample surface (250°C) using a liquid flow rate of 2 ml/min through a stencil mask to achieve rudimentary patterning. The total time for the cyclic spray deposition step was 10 min. For spin coating deposition of ZnO films, the precursor solution was formed by dissolving zinc oxide hydrate (ZnO·H$_2$O, 97%, Sigma-Aldrich) in ammonium hydroxide [50% (v/v) aqueous solution, Alfa Aesar] at a concentration of 10 mg/ml and stirred at room temperature for 2 to 3 hours. The spin coating parameters used for the spin coating of ZnO was 4000 rpm for 30 s. As-deposited films were subjected to thermal annealing at 210°C to 250°C for 30 min. All chemicals were used as received.

**Transistor fabrication and characterization**

Transistors were fabricated in bottom-gate, top-contact architecture on wafers of highly doped Si (Si$^{++}$) equipped with a 400-nm-thick thermally grown layer of SiO$_2$ acting as the gate electrode and the gate dielectric, respectively. The Si$^{++}$/SiO$_2$ wafers were cleaned by subsequent ultrasonication in DI water, acetone, and isopropanol for 10 min each, followed by ultraviolet/ozone treatment for 15 min. Deposition of the metal oxide layers was performed using the methods described above. Transistor fabrication was completed with the deposition of top Al S-D electrodes under high vacuum (~10$^{-6}$ mbar). The channel width (\(W\)) and length (\(L\)) of the resulting devices were 1000 and 100 \(\mu\)m, respectively. The electrical characterization of the transistors was carried out at room temperature in a nitrogen glove box using an Agilent B2902A parameter analyzer or at different temperatures in a cryogenic probe station (ST-500, Janis Research) under high vacuum (10$^{-5}$ mbar) using a Keithley 4200 semiconductor parameter analyzer. The field-effect mobility was extracted from the transfer characteristics in the linear and saturation regimes using the gradual channel approximation model

\[
\mu_{\text{LIN}} = \frac{L}{W C_i V_D} \frac{\partial I_{\text{D,lin}}}{\partial V_G}
\]

\[
\mu_{\text{sat}} = \frac{L}{W C_i} \frac{\partial^2 I_{\text{D,sat}}}{\partial V_G^2}
\]

where \(L\) and \(W\) are the channel length and width, respectively, \(C_i\) is the capacitance of the gate dielectric, \(V_D\) is the S-D voltage, and \(V_G\) is the gate voltage.

**Material characterization techniques**

Topography and roughness of semiconductor samples were measured via intermittent contact mode AFM (Agilent 5500 AFM system). A Titan 80–300 Super Twin microscope (FEI Company) operating at 300 kV and a JEOL 2011 electron microscope operating at 200 kV were used to perform HRTEM imaging and analysis. Two TEM sample preparation techniques were used as follows: (i) ion beam milling (Ga ion beam, 30 kV, and 9 nA) to cut a specimen from the bulk sample, which was then attached to a Cu grid in a lift-off method and further thinned down to ca. 50 nm thick and cleaned (2 kV and 28 pA) to remove areas that were damaged during the thinning process. Before the milling process, the sample surface was protected against ion bombardment via electron beam–assisted carbon and platinum deposition. (ii) The standard sandwich technique, followed by tripod polishing to reach a 30-nm-edge thickness. Electron transparency to less than 15 nm was achieved by precision low-voltage (5 to 1 keV) Ar$^+$ ion milling in a Gatan precision ion polishing system.

Core-level and VB XPS spectra were acquired in a KRATOS AXIS Ultra DLD system equipped with a monochromic AlK$_\alpha$ x-ray source, a hemispherical sector electron analyzer, and a multichannel electron detector. Depth profile analysis was performed by mild, destructive in situ sputter etching using a 500-eV defocused Ar$^+$ beam to achieve the required depth resolution. The XPS measurements were acquired using 20-eV pass energy, resulting in a full width at half maximum of the Ag-3d peak of less than 500 meV. Spectral shifts due to charging of the surface were evaluated and subtracted on the basis of the spectral positions of the C-1s of adventitious carbon and Ar-2p peak after sputter etching.

**SUPPLEMENTARY MATERIALS**

Supplemental material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/3/e1602640/DC1

**REFERENCES AND NOTES**


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Heterojunction oxide thin-film transistors with unprecedented electron mobility grown from solution
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