Selective control of electron and hole tunneling in 2D assembly

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Recent discoveries in the field of two-dimensional (2D) materials have led to the demonstration of exotic devices. Although they have new potential applications in electronics, thermally activated transport over a metal/semiconductor barrier sets physical subthermionic limitations. The challenge of realizing an innovative transistor geometry that exploits this concern remains. A new class of 2D assembly (namely, “carristor”) with a configuration similar to the metal-insulator-semiconductor structure is introduced in this work. Superior functionalities, such as a current rectification ratio of up to 400,000 and a switching ratio of higher than $10^6$ at room temperature, are realized by quantum-mechanical tunneling of majority and minority carriers across the barrier. These carristors have a potential application as the fundamental building block of low-power consumption electronics.

INTRODUCTION

Performance improvements have led state-of-the-art silicon-based electronics to face challenges in continuing to fulfill Moore’s law as a result of leakage current and electrostatic degradation (1). Fortunately, these challenges are expected to be met by an abundance of atomically thin, two-dimensional (2D) materials (2–4). Considering the natural advantages of 2D materials (3, 4), new transistor architectures could be realized by assembling diverse van der Waals materials into a 3D structure with superior performance in terms of the on/off ratio and the subthreshold swing. A popular van der Waals heterojunction, graphene/transition metal dichalcogenides (TMDs) (5–10), mimics a graphene barristor developed and named by Yang et al. (11) and has displayed Schottky-limited transport, revealing current on/off ratio values ranging widely from 10 to $10^3$ under the modulation of the Schottky barrier height $\phi_B$ (5–7, 9, 10). However, these devices have a critical weakness in the thickness of the active layer [TMDs or hexagonal boron nitride (hBN)], which exhibits either a strong temperature dependence or an uncontrollably small switching ratio. The off-state current $I_{OFF}$ is especially pronounced and is conceptually comparable to that of the conventional field-effect transistor (FET) (5, 6, 8, 11, 12) because it eventually results in either direct tunneling transport in thin devices (similar to channel shrinkage in FETs) (9, 10, 13) or thermionic emission transport with a thick active layer (long channel) by majority carriers (which are electrons in most devices) (7, 8, 11). Therefore, the challenge is to create and characterize a device that simultaneously has pure quantum tunneling transport in both the on and off states, a weak temperature dependence, and fast switching.

As a promising approach for achieving these goals, a metal-insulator-semiconductor (MIS) capacitor-like device is developed by sandwiching an insulating hBN tunnel barrier between a multilayer graphene (MGr) and an n-type tungsten disulfide (WS$_2$) nanosheet. Device operation relies on the tunability of the surface potential $\phi_S$ of WS$_2$ at the atomically abrupt interface that is switchable between the inversion of holes and accumulation of electrons, as controlled by the tunneling process across the insulator (Fig. 1A). Thus, a high current on/off ratio is robust for the controllability of $\phi_S$ by means of a Fermi level shift $\Delta E_{FG}$ in the electrostatically gated MGr. To date, a triode device based on band-to-band tunneling currents via the transition from minority to majority carriers has not been achieved; thus, we refer to our device as a “carristor” to reflect the carrier-controlled nature of the device. We have demonstrated that the proposed carristor (denoted below by MIS-C) can be created when the hBN thickness is intentionally reduced for operations away from thermodynamic equilibrium (Fig. 1B and fig. S1). In the overall study, we also fabricated alternative devices (barristors) composed of MGr-TMDs (denoted by GW-B and GM-B for WS$_2$ and MoS$_2$ active layers, respectively) for systematic comparison.

RESULTS

Figure 1C shows an optical image of one of the investigated carristors fabricated on a thermally oxidized 280-nm-thick layer of SiO$_2$ on a Si substrate (fig. S2). Briefly, a vertically assembled MGr-hBN-WS$_2$ stack was generated by the dry transfer of exfoliated nanosheets from individual bulk crystals and sandwiched by electrodes, namely, top (T1 to T3) and bottom (B) leads, to establish electrical interconnections. The details of the tunneling device fabrication procedure and the material characterization are presented in Materials and Methods. High-resolution transmission electron microscopy (TEM) allows us to verify the atomic sharpness of the interface (Fig. 1D), with a thin uniform tunnel layer of approximately 3 nm appearing both in the magnified TEM image and in the statistical histogram (for hBN/SiO$_2$ steps) acquired from atomic force microscopy (AFM) (Fig. 1, E and F). To construct the band lineup in the heterostructures, a conventional x-ray photoelectron spectroscopy (XPS) technique was used, which reveals a straddling heterojunction (Fig. 1G and fig. S4). When performing electrical transport measurements, the degenerately doped n$^+$-type silicon acted as a back gate for the modulation of $V_G$, and a dc bias voltage $V_{TB}$ was applied to one of the top leads while measuring the vertical tunnel current flow $I_{TB}$ (B is ground).

Carrier transport through the MIS system is often regarded as a leakage current in FETs (1, 14, 15). However, Fig. 2A shows that such a current becomes useful when a $V_{TB}$ value between $-3$ and $3$ V is applied. The output curve reveals strong asymmetric behavior that has characteristics analogous to that of a p–n junction diode or a typical Schottky diode. Therefore, the Shockley diode equation $I_{TB}(V_{TB}) = I_0[\exp(eV_{TB}/k_BT) - 1]$ can be used for quantitative characterization, where $I_0$, $e$, $k_B$, and $T$ are the saturation current, the elementary

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charge, the ideality factor, the Boltzmann constant, and the absolute temperature, respectively. In this way, a rectification ratio \( R_0 \) of approximately 100,000 and \( \eta = 1.2 \) can be calculated. The \( R_0 \) value obtained in our carristors represents at least a 10,000-fold improvement compared to other works investigating a p-n junction based on layer-by-layer stacked TMDs (16). We note that GW-B and GM-B performed within the limit in \( R_0 \) with a typical range of \(<10^2\) (fig. S5), which is consistent with previous reports (6, 7, 9). The \( \eta \) value was found to be much smaller than that of TMD-based barristors (6), implying an optimal interface density of states (DOS) at the hBN-WS2 interface. Such remarkable enhancements are expected to be a consequence of the substantial differences in the underlying principles of device physics.

The current rectifying behavior can be understood by examining the inset of Fig. 2A for \( V_{TB} > 0 \) (electron accumulation mode) and \( V_{TB} < 0 \) (hole inversion mode) biasing. The associated surface carrier density plot shown in Fig. 2B is consistent with this surface mode transition (see the Supplementary Materials for the calculation). Inversion- and accumulation-induced quasi-bound states, together with quantum confinement in the narrow quantum well near the WS2 interface, were not characterized in this work but are probably the cause of the momentum-conserved transmission phenomenon. This part of the field is still relatively unexplored.

Although the electron wave function can penetrate a several-atom-thick hBN barrier resulting in a tunneling phenomenon due to barrier height \( \Delta E_{1p} \) being much larger than the thermal energy, the conduction mechanism still needs to be elucidated and demonstrated using temperature-dependent transport measurements, as shown in Fig. 3A (the corresponding output data for GW-B are shown in fig. S6). The nearly flat out-of-plane resistivity of \(~10^8\) ohm\( \cdot \)cm (defined as \( R = 1/\left(dJ_{TB}/dT\right)\)), where \( J_{TB} \) is the current density) with decreasing temperature observed in Fig. 3B (MIS-C, blue squares) clearly indicates the tunneling behavior under the overall bias (10, 14). Alternatively, GW-B (yellow squares) shows a significant decrease in \( \rho \) by more than four orders of magnitude from 230 to 90 K with semiconducting behavior and from 245 K to room temperature with strong metallic behavior. These two temperature regimes have also been observed by Georgiou et al. (5). Metal-semiconductor contact could be responsive- adapted for the barristor and has indeed been extensively described by thermionic emission (6–8, 11), thermionic field-emission (8), and FET models (8). Figure 3C presents an Arrhenius plot of \( \ln(J_{TB}) \) versus \( T^{-1} \) for the carristor (blue) and the barristor (yellow). It is interesting to note that that MIS-C has an ultralow activation energy \( E_A \) of 13 meV that is evidently smaller than \( k_B T \) (\( T = 300 \) K). \( E_A \) has a certain correlation with the temperature-dependent on/off ratio. The current component, owing to the disorder-assisted generation-recombination (G-R) effect in the depletion region (with width \( W_D \)) governed by Shockley-Read-Hall statistics, is expected to be temperature-sensitive (14) because it is proportional to \( e\alpha(T)W_D^2/\tau \), where \( \tau \) is the carrier lifetime and \( n_i(T) \) is the intrinsic carrier density (see the Supplementary Materials). The measured \( E_A \) of the MIS-C is 100 times smaller than the half bandgap of WS2; thus, the insignificant generation of G-R current is suggestive (17). We attribute the nonzero \( E_A \) to the
bandgap reduction with temperature because of the intensified electron-phonon interaction at high temperatures that may alter the height of the barrier. More surprisingly, the external electric field resulting from the silicon back gate determines the output characteristics. Figure 3D presents representative $I_{TB}-V_{TB}$ curves for a $V_G$ range of $-7$ to $7$ V, allowing us to obtain $R_B$ versus $V_G$ over a range of 10 to 400,000 (inset of Fig. 3E). The nonlinear $I$-$V$ curves are divided into two distinctive signatures, namely, current multiplication for $V_{TB} < 0$ and a plateau pattern for $V_{TB} > 0$. When $V_{TB} < 0$, we observed a marked current enhancement by more than five orders of magnitude. When $V_{TB} > 0$, as $V_G$ is increased, a plateau can be clearly observed for each curve near zero $V_{TB}$ that becomes more pronounced at large positive $V_G$. This plateau corresponds to the raising of the depletion layer in WS$_2$ that is, it provides evidence of $(V_{TB}, V_G)$-dependent $\phi_e$. We note that a flat form of $\phi_e$ weakens the generation of electron density at the WS$_2$ surface, leading to a nearly constant current region. Moreover, as $\phi_e$ departs from the flat band to shift down as $V_{TB}$ increases, a large population of electrons allows all the curves to converge for a finite transmission coefficient $T_E$ (18). We hypothesize that $V_{TB}$, $V_G$, variations in $\phi_e$, and (constant) $T_E$ play major roles in our MIS-C, as will be discussed in more detail. Generally, the amount of surface DOS acts as G-R centers and as an extra tunneling path between graphene and WS$_2$. Green et al. (18) have shown that the influence of surface DOS is substantial when the MIS-C is positively biased. However, the existence of a plateau confirms that the localized DOS has no detectable effect on the bandgap of the semiconductor, consistent with a recent study by Braga et al. (19). By contrast, GW-B and GM-B do exhibit current multiplication behavior (figs. S7A and S8A) that has been observed in other studies, but such behavior lacks the current-plateau feature.

Charge transport in MIS structures has been studied extensively because it is related to the planar MISFET (metal-insulator-semiconductor field-effect transistor) and is of primary importance to the reliability and stability of integrated circuit technology. By incorporating the Wentzel-Kramers-Brillouin approximation for rectangular barrier, the expression for the band-to-band current $I_{TB}(V_{TB}, V_G) \propto T_E \exp\left[-\phi_e(V_{TB}, V_G)/k_B T\right]$ was used to analyze the characteristics of the MIS-C (see the Supplementary Materials). We note that the MIS-C mimics the conventional MIS capacitor in that the band bending effectively depends on work function difference $\phi_{m0}$ as mentioned above. Notably, we could electrostatically adjust the work function of graphene $W_G$ to generate an undoubted transition in $\phi_e(V_{TB}, V_G)$. It appears more directly, as displayed in Fig. 3E (left axis). Remarkably, by sweeping the polarity of $V_G$, $\phi_e$ can be sensitively changed from 92 meV at $V_G = -7$ V to $-205$ meV at $V_G = 7$ V, suggesting the significant influence of $\phi_e(V_G)$ to form hole inversion and electron accumulation (see the Supplementary Materials for the $\phi_e$ extraction method). However, in the case of the GW-B, a positive value of $\phi_{m0}$ (from 459 to 313 meV) can be found over the entire range of $V_G$ because the majority carrier transport is restricted only by $\phi_b$ (7–9, 11). This finding for the GW-B complies with theoretical predictions (20, 21) and experimental observation (10).

We define a barrier function $U_T = \ln(A^* A T^{2 T B})$, where $A^*$ and $A$ are the Richardson constant and active contact area, respectively. Figure 3F shows that the measured value of $U_T$ in our MIS-C is nearly independent of gate modulation at room temperature. Assuming the effective mass of a hole in hBN, $m_{BN}^* = 0.5 m_0$ (13, 22, 23), and taking barrier thickness $d_{BN}$ to be 2.8 nm, the theoretical model describes a calculated $U_T$ (red circles in Fig. 3F) close to the measured value without the gating dependence, as expected, demonstrating an effective $d_{BN}$ that is slightly smaller than $\sim 3$ nm (Fig. 1E). This observation reflects the lowering of the hole barrier behavior. Recent experimental efforts on tunnel devices with an hBN barrier embedded within different electrodes (graphene, graphite, and metal) have revealed discrepancies. The pronounced negative differential resistance with momentum transfer by aligning the crystal orientation of two graphene (24, 25) or defect-assisted (26) Coulomb blockade signatures with defect-mediated tunneling (27) and that of the sublinear $I$-$V$ curve with direct tunneling (22) is relatively ambiguous, although some of these devices contain identical graphene electrodes. Nevertheless, we did not observe resonant tunneling or single-electron charging effects in our samples; $T_E$ exhibited the expected behavior of exponential dependence on $d_{BN}$ and negligible barrier deformation as a function of $V_G$ (see the Supplementary Materials).

We now explore the “transistor-like” operation of the MIS-C for the first time. Figure 4A illustrates the transfer characteristics ($I_{TB}-V_G$)
for a typical sample measured at $V_{TB} = -0.5$ V. A linear scale $I_{TB}$-$V_{TB}$ plot with various $V_{TB}$ is displayed in the inset of Fig. 4A. We find that $I_{TB}$ has an exponential dependence on $V_G$ and a high on/off ratio of $3.6 \times 10^6$ at $V_{TB} = -0.5$ V even at room temperature (see fig. S10 for different $V_{TB}$ voltages), which is 100 to 100,000 times higher than the values reported in previous reports of graphene/TMD-based barristor (see figs. S7B and S8B for the results of our barristors) (5–7, 9–11, 13). Figure 4B depicts the corresponding asymmetric variation in $D_{FG}$ as a function of $V_G$. The asymmetry is probably caused by the unbalanced hole doping because the carrier counteraction occurs between the hole carriers doped by the negative polarity of $V_G$ and the small amount of electron carriers created by negative $V_{TB}$ (note that charge neutrality requires an equal charge at both sides of the semimetal and the semiconductor) (14). In addition, the preceding discussions assumed the ability to control the sequential tunneling of the double carriers. To further address this point, we fabricated MGr-based conventional FETs on SiO$_2$/Si wafer. The inset of Fig. 4C (top right) shows an optical image of the MGr-FET. A linear output behavior [inset of Fig. 4C (bottom)] confirms metal-to-MGr contact before in-plane resistivity $r$ analysis. The associated $r$ as a function of $V_G$ presented a peak at the Dirac point voltage corresponding to the vanishing of the DOS as $E_F$ approached the Dirac point (Fig. 4C). Although different MGr FETs display different peak positions due to oxide charges and unintentional doping, the $E_F$ of MGr crosses over to the Dirac point (28, 29). This behavior is similar to that of single-layer graphene (28).
should also be available. The electrostatic gating from the Si substrate is effectively screened by MGr \(^{(29, 30)}\) and do not generate n- or p-doping in MGr. \(I_{\text{off}}\) and the on-state current \(I_{\text{on}}\) are similar to the current corresponding to negative and positive \(V_{\text{TB}}\), respectively. The inset of Fig. 4D shows a plot of \(\ln\left(G_{\text{on}}/G_{\text{off}}\right)\) vs. \(1000T^{-1}\) in both on and off states, indicating that the observed behavior is in agreement with that of Fig. 3A. By using \(\ln\left(I_{\text{on}}/I_{\text{off}}\right) \propto -E_A/k_B T\), the measured \(E_A\) in Fig. 4D (red squares) corresponds to approximately 11 meV, which is very close to the data extracted from Fig. 3C. In contrast, the GW-B exhibits an exponential decay with \(T\) (black circles) and a similarity in the decay slope to the results of other barristors \((5, 6, 9, 11)\). Their \(I_{\text{off}}\) response to temperature is analogous to the subthreshold conduction of silicon MISFETs \((12)\). The expression \(\ln\left(I_{\text{on}}/I_{\text{off}}\right) \propto -e\phi_g/k_B T\) is valid for describing Fig. 4D for barristors \((31)\). We could roughly extract \(e\phi_g\) of the barristors; typical values lay in the range of 148 to 303 meV.

**DISCUSSION**

To summarize, assembly of 2D crystals with atomic precision enables the creation of a novel carristor via layer-by-layer construction with materials having a distinctive electronic structure. Our assembly, the so-called carristor, exhibits current rectification and switching features and could open new routes for constructing electronic devices by taking advantage of the small active area (lack of double contact space...
for S/D) and ultrafast direct tunneling time, which could enable the direct rectification of infrared radiation.

**MATERIALS AND METHODS**

**Device fabrication**

For the vertically stacked MGr-hBN-WS2 (MIS-C) and MGr-TMD (GW-B and GM-B) devices, we used the standard Scotch tape-based cleavage technique for each 2D bulk crystal in combination with a contamination-free transfer method to avoid wet chemicals and even deionized water (32, 33). Single-crystalline graphite was purchased from Graphene Supermarket, and hBN, WS2, and MoS2 were purchased from 2D Semiconductors. First, the bottom contact was prepared onto a degenerately doped Si substrate, followed by a 280-nm-thick SiO2 capping layer, as shown in fig. S2A. Then, we applied mechanical exfoliation to obtain a MGr nanosheet that was deposited on a polydimethylsiloxane (PDMS) layer. Thick pieces of graphene with a typical thickness of 10 to 27 nm were chosen to create the bottom contacts, fully suppressing any underlying electric field screening (screening length of 1.2 nm) (29, 30). This intermediate PDMS layer acted as a supporting framework for the transfer of 2D nanosheets by means of a micro-manipulation system (33). After the MGr was placed at the desired location on the silicon substrate, we transferred an hBN nanosheet so that it overlapped the underlying MGr flake (fig. S2B). Subsequently, the top layer (WS2 nanosheet) was placed onto the high-quality hBN that was used as both a tunnel barrier and an ultrasmooth, defect-free substrate (fig. S2C) (34). A 1.4-μm-thick layer of negative-tone photoresist was spin-coated on the sample and patterned using a photomask through a photolithography process (fig. S2D). We metallized three separate top Ti/Au (10/60 nm) contacts for the vertical device using a thermal evaporator with a deposition rate of 5 Å/s. GW-B and GM-B have the same fabrication procedures but without inserting an hBN tunnel barrier for the direct MGr-TMD contact (fig. S3, A to D). Dozens of devices were fabricated and studied in the process of completing this study.

**Materials characterization**

High-resolution TEM images were obtained with a JEOL JEM-2100F operating at 200 kV. Before the TEM analysis, a focused ion beam (Quanta 3D FEG, FEI) was used to prepare site-specific samples (inset of Fig. 1D). The focused ion beam cutting and lift out were performed after the deposition of a carbon/PT coating. The cross-sectional specimen was extracted from the studied device and used to determine the individual thicknesses of the layered materials and to verify the atomic sharpness of the interfaces. Topographic image and histogram statistics were carried out using an AFM (XE-100, Park Systems) in the noncontact mode of operation with an AR5-NCH (Nanosensors) cantilever. XPS core-level and valence band spectra were collected using an XPS (angle-resolved XPS, Thermo Fisher Scientific), incorporating a monochromatic Al Kα source (1486.6 eV). Energies of the spectra were calibrated against the C 1s peak at set to 284.5 eV.

**Electrical measurement**

$I$–$V$ characteristics were conducted using a semiconductor parameter analyzer (HP 4156A) and measured in a liquid nitrogen–cooled cryostat (ASK, 700 K) at a pressure of approximately $10^{-5}$ torr in a dark environment.

**SUPPLEMENTARY MATERIALS**

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/4/e1602726/DC1

**Supplementary Text**

fig. S1. The 3D schematic structure of the carriost.

fig. S2. Optical images of MIS-C fabrication steps.

fig. S3. Optical images of GW-B (or GM-B) fabrication steps.

fig. S4. Band alignment of MIS-C and XPS spectra.

fig. S5. Schematic representation and $I$–$V$ curves.

fig. S6. $I$–$V$ curves for experimental (black line) and calculated data (red dots) under zero gate field and $T = 300$ K.

fig. S10. Semilog $I$–$V$ curves for MIS-C at different $V_{TS}$ from $-0.1$ to $-0.5$ V at room temperature.

**REFERENCES AND NOTES**


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