Nondestructive imaging of atomically thin nanostructures buried in silicon

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It is now possible to create atomically thin regions of dopant atoms in silicon patterned with lateral dimensions ranging from the atomic scale (angstroms) to micrometers. These structures are building blocks of quantum devices for physics research and they are likely also to serve as key components of devices for next-generation classical and quantum information processing. Until now, the characteristics of buried dopant nanostructures could only be inferred from destructive techniques and/or the performance of the final electronic device; this severely limits engineering and manufacture of real-world devices based on atomic-scale lithography. Here, we use scanning microwave microscopy (SMM) to image and electronically characterize three-dimensional phosphorus nanostructures fabricated via scanning tunneling microscope–based lithography. The SMM measurements, which are completely nondestructive and sensitive to as few as 1900 to 4200 densely packed P atoms 4 to 15 nm below a silicon surface, yield electrical and geometric properties in agreement with those obtained from electrical transport and secondary ion mass spectroscopy for unpatterned phosphorus 6 layers containing ~10^{13} P atoms. The imaging resolution was 37 ± 1 nm in lateral and 4 ± 1 nm in vertical directions, both values depending on SMM tip size and depth of dopant layers. In addition, finite element modeling indicates that resolution can be substantially improved using further optimized tips and microwave gradient detection. Our results on three-dimensional dopant structures reveal reduced carrier mobility for shallow dopant layers and suggest that SMM could aid the development of fabrication processes for surface code quantum computers.

INTRODUCTION

Semiconductor nanostructures consisting of areas of buried dopant atom(s) are crucial components for present and future complementary metal-oxide semiconductor transistor technologies (1), as well as for emerging quantum computing architectures (2, 3). Depending on their size and shape, they can produce quantum confinement in one, two, or three dimensions, which may be exploited for device operation. Consequently, noninvasive imaging and electrical characterization of buried nanostructures, with precise lateral and depth resolution, would be of great value for the development and inspection of integrated circuits and quantum devices.

Over the last decade, the technique of hydrogen resist lithography, which uses a scanning tunneling microscope (STM) to pattern a hydrogen passivation layer, has proved ideal for the definition of laterally confined atomically thin two-dimensional (2D) phosphorus (P) dopant nanostructures. Nanoscale P sheets (4), wires (5), and dots (6) have all been fabricated. These buried nanoscale structures challenge techniques aimed at determining electrical and geometrical properties of subsurface devices. STM itself offers only limited subsurface sensitivity (7) for imaging and no ability to determine the sheet resistivity of the nanostructures or their depth beneath the surface. In contrast, scanning probe microscopy techniques based on applying alternating electric fields and probing the local impedance are more useful for subsurface imaging because the field penetrates further. Established methods such as electrostatic force microscopy (EFM) and scanning capacitance microscopy, measure capacitances at kilohertz and megahertz frequencies and are capable of imaging subsurface features (8–10); however, the data provide only qualitative image contrast. Here, we show that scanning microwave microscopy (SMM), which operates at higher frequencies (1 to 20 GHz) and can measure the complex impedance of the buried nanostructures, gives access to both dielectric (11–14) and conductivity (15–17) properties, including, in particular, those due to dopants (16, 18–21). Unlike destructive imaging techniques such as focused ion beam milling combined with scanning electron microscopy (22), transmission electron microscopy (TEM) (23), and secondary ion mass spectrometry (SIMS) (24), SMM experiments can be performed with virtually no sample modification, in an ambient environment, using a standard atomic force microscope (AFM) (25) or STM (26) combined with a vector network analyzer (VNA) (27) or custom-made electronics (28). Typically, resonators (29) or matching circuits (28), as well as simpler direct connections (30, 31), are used to sense the minute electrical changes that come from the SMM probe. Recently, it has been shown that SMM is capable of visualizing buried conducting structures (20, 21, 32) and differently doped bulk regions buried below an insulating layer (33). Here, we demonstrate the capability to determine the 3D disposition and electrical characteristics of atomically thin buried phosphorus nanostructures formed by incorporation and encapsulation of substitutional P atoms within multiple layers in a Si crystal. Using optimized growth parameters, the layers are densely packed (1.4 atoms/nm^2) and can be confined to widths of a few nanometers, with near 100% carrier activation, within the confined region (34). The capabilities demonstrated here are transformative for noninvasive diagnostics of atomic-scale electric components that will form the next generation of “classical” and quantum devices.

Figure 1 shows the SMM setup, and Materials and Methods explains its operation. Briefly, a VNA connected to a conducting AFM probe transmits an electromagnetic wave to the probe and detects the reflected wave. The ratio of the incident and the reflected signal power (the...
complex $S_{11}$ reflection parameter) gives information on the local sample properties below the probe. High sensitivity to variations in the sheet resistivity of P dopant layers is obtained by operating the SMM at frequencies below the probe. High sensitivity to variations in the sheet resistance of buried phosphorus nanostructures forming local conducting planes below the surface such that a capacitance, $C = \varepsilon A/d$, is built up between the buried plane and the conducting probe apex, where $A$ is the physical contact area between the probe tip and the substrate surface, $d$ is the depth, and $\varepsilon$ is the Si dielectric constant. For the substrate, the measured capacitance must be lower because it is governed by the width of the depletion layer, which is much larger than the P-layer depth (for details, see section S2) (36).

For a quantitative interpretation, which is required to extract the exact depth of the phosphorus layer and its conductivity, this simple picture has to be refined by also taking into account the precise geometry of the system and the dopants in the substrate. We have used FEM to calculate the theoretical admittance of the model shown in Fig. 3A. The phosphorus is modeled as a thin layer (0.2 nm) with a conductivity, $\sigma _p$, embedded at a depth, $h$, in the depletion layer of the low-doped silicon substrate. The basis for the assumed layer thickness is justified by the data shown in fig. S1 and associated text. Further, we note that the 0.6 nm roughness increase in the desorbed hydrogen desorbed triangle in Fig. 2H shows no measurable capacitance signal is detected by a lock-in amplifier. Workflow for dopant depth extraction shown in (1) SMM $S_{11}$ images/curves are calibrated (13) to obtain quantitative complex admittance data, $Y = G + i\omega C$, with $C$ as the capacitance, $G$ as the conductance, $\omega$ as the angular frequency, and $p = -1$. (2) FEM is used to extract sheet resistance and depth from the admittance signal. RF, microwave signal.
Fig. 2. SMM imaging of patterned phosphorus δ layers buried via epitaxy on Si(100) wafers. (A) AFM topography after coverage with 15 nm of Si. (B) SMM capacitance image showing clear contrast for the phosphorus pattern. (C) SMM conductance image. Corresponding line profiles are shown in (D), (E), and (F), respectively. Line profile across the square pattern (black, single line; red, 10 lines averaged; blue, fit with logistic function). (G) AFM topography image of patterned phosphorus (P) layer and depassivated hydrogen (H) layer. Corresponding (H) capacitance and (I) conductance images. Scale bars, 1.4 μm; VNA power, 1 dBm; f = 19.81 GHz; scan speed, 0.4 lines/s (512 points).

Application to 3D P δ-layer structure

We have applied the SMM imaging capabilities to an advanced δ-layer structure, as shown in Fig. 4A. This complex structure consists of two overlaid perpendicular sets of three phosphorus-doped bars. Each set of bars was prepared in the same manner using three different PH₃ doses, one for each bar, leading to different doping densities as indicated. A separation layer of approximately 5 nm of Si was grown between the patterned sets of the bars, such that the overlaid sets of bars reside at depths of h = 8.9 nm and h = 4 nm below the surface (as verified by SIMS measurements on an unpatterned double δ-layer sample fabricated using the same growth parameters; see section S3 and fig. S4). The SMM measurements were carried out using a blunter tip (as shown in fig. S2B) giving a clearly larger capacitance, proving the importance of the precise tip geometry.

After having defined all the geometrical parameters in the model, the depth of the dopant layer and its conductivity can be extracted by comparing the experimental capacitance and conductance images (Fig. 2) with the simulated values. Therefore, in Fig. 3 (E and F), the simulated capacitance and conductance differences (P δ-layer ground plane minus substrate) are shown as a function of the phosphorus layer conductivity for dopant depths of h = 15 nm (solid line and h = 10 nm/20 nm, respectively (dotted lines). The experimentally obtained values are shown as red dots and result in a dopant layer depth of h = 15 ± 1 nm and a conductivity of σ₁ = 1.2 × 10⁶ S/m. Although the SMM measurement frequency has been chosen for sensitivity to variations for the highly ( > 10⁵ S/m) conductive P dopant layers, the decreasing sensitivity at >10⁵ S/m (cf. Fig. 3, E and F, and fig. S1) leads to larger confidence intervals of (10⁵ to 10⁸) S/m. This is not surprising because it is in the metallic regime. However, by using larger tip radii (fig. S2B and Fig. 3G), we are able to decrease the confidence interval and extract h = 14 ± 1 nm and σ₂ = 3 × 10⁶ S/m with (2 × 10⁶ to 5 × 10⁶) S/m. Equalizing the simulated and measured complex admittance values means that two constraints have to be met, so that both phosphorus conductivity and dopant depth can be extracted clearly and without ambiguity. This can be observed also by the additional representation of the capacitance and conductance data in the complex plane for small (Fig. 3F) and large (Fig. 3G) tips.

Fig. 3C validates the initial assumption that, essentially, the entire potential drops off in the h = 15 nm between the tip and the buried phosphorus nanostructure. For the case where no phosphorus is present, the potential decays much more slowly within the substrate, leading to a lower capacitance. Because the size of the probe tip is just a few tens of nanometers, most of the potential in the depletion layer decays in the first few hundred nanometers below the surface, indicating that, for a few tens of nanometers, most of the potential in the depletion layer decays in the substrate, leading to a lower capacitance. Because the size of the probe tip is just a few tens of nanometers, most of the potential in the depletion layer decays in the first few hundred nanometers below the surface, indicating that, for small probe tips, the technique is most sensitive to the near subsurface, as also discussed in section S2 and by Fumagalli et al. (37) and Gramse et al. (38).

For a quantitative extraction of the dopant layer depth, the tip geometry and contact area between the conducting tip and sample are essential properties that need to be established experimentally. Therefore, we fit simulated capacitances to a capacitance versus distance curve on the bare Si substrate obtained directly after imaging the nanostructure (fig. S2). The free parameters in this fitting procedure are the apex radius, cone angle, and contact radius of the circular contact area, which are determined to be r_a = 20 ± 5 nm, θ = 8° ± 1°, and r_c = 11 ± 2 nm, respectively. The first two parameters are extracted from the out-of-contact region of the approach curve, whereas r_c is determined from the region where the tip is already in contact with the substrate (for details, see section S2). The extracted values are within the nominal 10- to 30-nm range of values provided by the tip manufacturer (39). Measurements carried out using a blunter tip (as shown in fig. S2B) give a clearly larger capacitance, proving the importance of the precise tip geometry.

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capacitance image in Fig. 4B shows a good contrast between the top and bottom levels, whereas the topography image is completely uncorrelated with the capacitance (see more details in fig. S5), except on bar B1 where the measurement has been hindered by surface modification during the lithography process. In particular, the bottom bar B3 shows a clear decrease in capacitance contrast (see line profiles in Figs. 4, C and D). The quantification of the dopant depth and concentration was carried out, as detailed above, but with a full 3D model (Fig. 4A). To this end, the experimental admittance data extracted from Fig. 4 (C and D) are plotted in Fig. 4E, together with the simulated values in the complex admittance plane. Note that we excluded bar B1 in this analysis because of the surface modification. The top levels agree well with a depth of $h_{T1} = 4.3 \pm 0.5$ nm, $h_{T2} = 4.5 \pm 0.5$ nm, and $h_{T3} = 4.2 \pm 0.5$ nm, and also the depth of bottom levels of $h_{B2} = 8.2 \pm 0.7$ nm and $h_{B3} = 9.6 \pm 0.7$ nm can be still extracted, however, with lower accuracy. The extracted conductivities are $\sigma_{B2} = (1 \pm 0.2) \times 10^{6}$ S/m and $\sigma_{B3} = (0.7 \pm 0.1) \times 10^{6}$ S/m and, for the top levels, $\sigma_{T1} = (0.7 \pm 0.1) \times 10^{6}$ S/m, $\sigma_{T2} = (0.65 \pm 0.1) \times 10^{6}$ S/m, $\sigma_{T3} = (0.62 \pm 0.1) \times 10^{6}$ S/m.

**Lateral resolution and sensitivity**

The sensitivity to buried and isolated P atoms and the capability to laterally resolve fine P patterns are two key features of the technique. The lateral resolution was derived from the capacitance line profile in Fig. 2E, which was fitted with a difference of two logistic functions, $f_{\logi}(x) = A (1 + e^{-(x-x_0)/\delta_A})^{-1} - A (1 + e^{-(x-x_1)/\delta_1})^{-1}$, where $A$, $\delta$, $x_0$, and $x_1$ are the fitting parameters and $\delta$ defines the sharpness of the step. From this fit, the width of the step from Si to P has been estimated to be $R_{\text{Si-PS}} = 28 \pm 55$ nm. For the shallower 3D structures in Fig. 4, we find an improvement to $\delta_B = 47 \pm 3$ nm for the bottom layer and $\delta_T = 37 \pm 1$ nm for the top layer, notwithstanding that we also used here a bigger tip radius to increase the accuracy of the extracted $R_{\text{sheet}}$.

From measurements on fine patterns (see fig. S6 and section S4), we found that isolated features as small as 10 nm buried at 15 nm can still be detected; however, they appear broadened in the capacitance image. To obtain a quantitative estimate of the feature size that can be resolved in more complex and dense circuits, five pairs of stripes with increasing pitch have been patterned (200, 150, 100, 70, and 30 nm) and buried below 15 nm of Si. The SMM capacitance image in Fig. 5A and the corresponding line profile in Fig. 5B demonstrate that the stripes separated by 70 nm can still be resolved, in agreement with the previous observation. At 30-nm separation, the SMM does not distinguish the individual stripes.

The fit of capacitance curves from 3D finite element simulations to the experimental data yielded the same apex but a slightly increased contact radius indicative for tip wear typically observed after prolonged scanning. Overall, the simulated data agree well with the experiment, and only at low separations, $L = 30$ to 70 nm, a minor difference between experiment and simulation is visible. The effect of the two parameters defining the lateral resolution, namely, the depth of the dopant layer, $h$, and the apex radius, $r_p$, has been modeled, as shown in Fig. 5 (C to F). For stripes with a pitch of 100 nm, the depth was varied from $h = 5$ nm to $h = 100$ nm, showing a clear increase (decrease) of the contrast for lower (higher) Si coverage, as expected. Assuming an SMM capacitance sensitivity of 0.5 aF (bandwidth, 25 Hz), the maximum resolvable feature separation, $L$, has been calculated from the data in Fig. 5C as a function of the depth. For a dopant depth of $h = 5$ nm, the SMM should clearly resolve separations of $d = 40$ nm, as we also observe in our experiments, whereas at $h = 40$ nm, it is expected to have only submicrometer lateral resolution, as can be seen in Fig. 5D. Simulations with varying tip radius in Fig. 5 (E and F) show that the lateral resolution does not increase monotonically with decreasing tip radius. There is rather an optimum contact radius, which is in the range of 30 to...
DISCUSSION

We have demonstrated SMM, which combines AFM as a nanoscale investigation technique and the VNA for quantitative microwave measurements, to be an excellent tool for locating and investigating buried electronic features. The novel characteristics of the technique are that it is noninvasive, enables location of features in three dimensions with high resolution, and provides their quantitative electrical characteristics. In particular, atomically thin layers of phosphorus, patterned by STM hydrogen desorption lithography and buried below 15 nm of Si, are easily resolvable and quantitatively characterizable using SMM. These layers are known to form subsurface 2D electron gases exhibiting quasi-metallicity and weak localization (42, 43); determining their sheet resistance via ordinary dc techniques is challenging because of the need to establish the appropriate electrical contacts and is even more difficult at room temperature where other current paths contribute to the electrical transport. The extracted depth of 14 ± 1 nm and sheet resistance of $R_{\text{sheet}} = 1.7 \pm 0.7$ kilohms per square compare favorably with similar values measured for phosphorus δ-layer samples fabricated in an identical way but without the H lithographic step (see Materials and Methods). SIMS measurements on these samples determined a depth of 14.45 ± 0.01 nm. Hall bar measurements, also made on the unpatterned samples, measured a sheet resistance of 1.4 ± 0.1 kilohms per square.

The application of SMM to more complex 3D structures consisting of two layers separated by only 5 nm shows the practical use of the technique to assess the quality in terms of electrical conductivity and distinguish different doping levels and depths of the δ layers. The extracted depth of both layers $h_B = 8$ to 10 nm and $h_T = 4$ nm shows a very good agreement with SIMS measurements (see Fig. S4). Although the maximum P density is identical to the one used in measurements of Fig. 2, for the 3D sample, we observe an $R_{\text{sheet}}$ of 5 to 8 kilohms per square, which is significantly higher than on the single-layer sample buried below 15 nm of Si. On the one hand, this quantitative difference in $R_{\text{sheet}}$ might suggest a reduced P activation and/or Si homogeneity that is expected because of the more complex preparation procedure, which includes the use of locking layers (44). On the other hand, our results would support the findings of Clarke et al. (45), which suggest a 40% lower carrier density from carriers located at dopants closer to the surface (4 nm) compared to those at 9 nm. The latter explanation would...
assuming averaged) including simulated capacitance for corresponding phosphorus stripes assuming $h = 15$ nm depth below surface, apex radius $r_a = 20$ nm, and contact radius $r_c = 12$ nm (VNA power, 1 dBm; $f = 19.05$ GHz). (C) Simulated capacitance profile for phosphorus structure at $h = 5, 15, 30$, and 100-nm depth (separation, $L = 100$ nm). (D) Resolvable P feature separations as a function of the layer depth (for an SMM sensitivity of 0.5 aF). (E) Normalized simulated capacitance profiles of P stripes in dependency of contact radius ($L = 100$ nm), au, arbitrary units. (F) Normalized capacitance contrast from (E) as a function of contact radius $r_c$. (Note that $r_t = r_a$ to reduce the number of parameters).

Fig. 5. SMM capacitance subsurface lateral resolution. (A) SMM capacitance image of stripes and (B) corresponding capacitance line profile (black dots, 10 lines averaged) including simulated capacitance for corresponding phosphorus stripes. (C) Simulated capacitance profile for phosphorus structure at $h = 5, 15, 30$, and 100-nm depth (separation, $L = 100$ nm). (D) Resolvable P feature separations as a function of the layer depth (for an SMM sensitivity of 0.5 aF). (E) Normalized simulated capacitance profiles of P stripes in dependency of contact radius ($L = 100$ nm), au, arbitrary units. (F) Normalized capacitance contrast from (E) as a function of contact radius $r_c$. (Note that $r_t = r_a$ to reduce the number of parameters).

be supported by the fact that the bottom layers show a lower $R_{\text{sheet}}$ and a stronger dependency on the applied P doses than the top layers.

Our results indicate that the SMM technique is capable of detecting a region of patterned phosphorus (P) with as few as 1900 or 4200 densely packed atoms, buried 4 or 15 nm below the silicon surface, respectively. Because we are sensing the capacitance formed between the tip and the P layer, we expect the sensitivity to scale inversely with the depth of the structures, implying that of order $10^3$ P atoms, corresponding to an area of $25 \times 25$ nm$^2$, can be detected at a 1-nm depth, and $10^4$ atoms at 100-nm depth (see fig. S6). These are remarkably small numbers, given that the sample does not have to be destroyed to achieve the measurement, as is the case for TEM or atom probe tomography. Other techniques, such as SIMS, which is generally regarded as a highly sensitive element-specific technique, cannot be used at all to measure the properties of these buried nanostructures. As mentioned earlier, the scanning dc or low-frequency capacitance microscopy technique can potentially image the same number of dopants; however, it cannot provide the depth and electrical information of SMM. The current interest in noninvasive imaging is highlighted by a very recent paper, which describes the use of a near-field terahertz imaging technique to image a printed circuit board on the underside of a 115-µm-thick silicon wafer (46). However, the technique only has a lateral resolution of ~100 µm, over three orders of magnitude coarser than the SMM.

The results presented here open up exciting opportunities for dopant nanostructure fabrication by providing a measurement capability not possible with any other technique. Besides localizing dopants in three dimensions, SMM accesses the intrinsic electrical properties of the δ layers. In addition, being nondestructive, it can be implemented within the same scanning probe instrument used to pattern the devices, which allows in situ and iterative control during the entire lithography/molecular beam epitaxy (MBE) process for atomic-scale deterministic doping. This ability will be especially useful to speed up the current development of 3D patterned device structures (47) and significantly aid in the interpretation of their electrical transport behavior. One of the several exciting applications that could emerge from our research is the use of SMM as a diagnostic for the development of a surface code quantum computer (SCQC) (2, 3). In the SCQC proposed by Hill et al. (2), the single dopant qubits are manipulated and read out using single-electron transistors (SETs) and a crossbar array of electrodes. Both the SETs and the arrays are fabricated from precisely placed arrays of dopants, below the silicon surface, on three separate layers. With further expected improvements in the SMM technique, direct imaging SETs and electrodes would be possible.

**MATERIALS AND METHODS**

**Sample preparation**

The P δ-layer nanostructures were fabricated using an Omicron VSTM system with a base pressure of less than $2 \times 10^{-10}$ mbar. Samples with a size of $9 \times 2$ mm$^2$ were diced from an n-type arsenic-doped Si(100) wafer (15 Ohm-cm and 500 µm in thickness). The Si surface was cleaned and passivated with hydrogen in ultrahigh vacuum using a standard process (41). Briefly, patterns of clean Si were written by depassivating the Si(100)-2 × 1:H surface (48) using the electron beam from an STM tip. Exposing the patterned surface to a background PH$_3$ pressure of $\approx 1 \times 10^{-9}$ mbar for 2 min [0.09 Langmuir (L)] resulted in adsorption of the PH$_3$ molecules exclusively within the depassivated regions (49). The phosphorus atoms were incorporated into the surface via a 2-min anneal at 350°C (40), and subsequently the donor nanostructure was encapsulated with 15 nm of silicon, grown by MBE from a Si sublimation source. A low sample temperature of $\approx 250$°C during the Si sublimation provided both a low donor surface segregation and relatively smooth Si crystal growth (35).

The 3D P δ-layer structure had been fabricated using a similar method to that used for the first sample. After depassivating an area of $3.5 \times 0.5$ µm$^2$ for the first bar, the surface was exposed to a PH$_3$ saturation dosage of 0.09 L. This procedure was subsequently repeated for the second (0.003 L) and third (0.002 L) bars. After an incorporation anneal for 2 min at 350°C, the sample had been encapsulated with 5 nm of silicon. For the first 10 monolayers the sample temperature was kept at low temperatures (around 60°C) to suppress P segregation [the use of a so-called “locking layer,” as described by Keizer et al. (44)], followed by a rapid thermal anneal of 15 s at 500°C and a lower silicon encapsulation temperature of 250°C with a rate of 1 monolayers per minute. After reaching the estimated final encapsulation thickness of 5 nm, a 2-min anneal to 450°C led to a low surface roughness, ensuring a high-quality H passivation for the second δ-layer patterning. The bars in the top layer had been written and dosed with...
the same parameters as those in the bottom layer but were rotated by 90°.

Growth calibration by δ-layer samples
To establish appropriate growth parameters, we performed a separate series of sample preparation and characterization steps on phosphorus δ-layer samples: These were the samples where an entire substrate was exposed to phosphine without any H passivation or lithographic patterning steps. The samples were overgrown with 15 nm of epitaxial silicon in the same way as for the nanostructured samples.

SIMS measurements on these δ-layer samples determined the thickness of the Si capping layer to be 14.45 ± 0.01 nm. Hall bar measurements of buried active P δ layers grown using the same PH3 background pressure and exposure time determined a sheet dopant density of (2.87 ± 0.03) × 10¹⁴ cm⁻² for a PH3 saturation dosage of 0.09 L, (6.23 ± 0.03) × 10¹³ cm⁻² for a dose of 0.003 L, and (1.86 ± 0.03) × 10¹⁵ for a dose of 0.002 L, respectively, which is consistent with previous reports (40). These values corresponded to donor densities of (4.7 ± 0.05) × 10²¹ cm⁻³, (1.0 ± 0.05) × 10²¹ cm⁻³, and (0.3 ± 0.05) × 10²¹ cm⁻³, respectively.

SMM setup and calibration
A commercial transmission line SMM consisting of a standard 5600 AFM interfaced with a 20-GHz VNA was used (both from Keysight Technologies). Soft (k = 0.3 N/m) solid platinum AFM tips (Rocky Mountain Nanotechnology) were chosen to reduce the contact force and maintain a sharp tip. The AFM tip was used as a nanoscale imaging and microwave probe, enabling simultaneous topographic and electromagnetic characterization of the sample. We used contact mode for the xy scans reported in this paper. The VNA measured the ratio of the incident and the reflected signal at the tip, the so-called scattering S₁₁ parameter. To transform the high impedance of the tip-sample contact to the sensitive 50 ohms of the VNA, a half-wavelength coaxial resonator in conjunction with a 50-ohm shunt resistor was used (50). Measurements were performed at frequencies between 18 and 20 GHz.

To convert measured reflection S₁₁ values into capacitance values, we applied the calibration procedure recently proposed by Gramse et al. (13). The measured reflection coefficient S₁₁ was converted into the complex impedance Z using the one-port black-box calibration. The defined calibration standards to calculate three complex error parameters ε₀₀, ε₀₁, and ε₁₁ were provided by simultaneously acquiring EFM and S₁₁ approach curves. For this, the tip approached the surface until it made contact, and both the EFM-dC/dz and the S₁₁ signals were recorded. No external capacitance calibration sample was required. The main advantages of this approach are that it works in situ on the sample under test, making a specific calibration sample redundant.

REFERENCES AND NOTES

SUPPLEMENTARY MATERIALS
Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/6/e1602586/DC1
section S1. Selection of measurement frequency
section S2. Fem for the extraction of conductivity and depth of dopant layer
section S3. Dopant distribution
section S4. Lateral/vertical resolution and sensitivity
fig. S1. Frequency sensitivity analysis.
fig. S2. SMM approach curve for electrical tip calibration.
fig. S3. Finite width of 2D-layer distribution.
fig. S4. SIMS measurement of phosphorus and oxygen on a 3D sample for verification of dopant depth.
fig. S5. Topography and SMM capacitance image of 3D sample.

fig. S6. Lateral resolution from STM and SMM capacitance.
fig. S7. Lateral SMM capacitance resolution for increasing tip radii.


Acknowledgments: M. Kasper, S.-S. Tuca, and L. Michalas are acknowledged for helpful technical discussions. Funding: This work has been supported by the European Union Seventh Framework Program (Marie Curie Initial Training Network NANOMICROWAVE, PEOPLE-2012-FP7-117116), the Austrian Research Promotion Agency (FFG, Bio-SMM project 846532), Austrian Science Fund (FWF, project P28018-S2), and the Engineering and Physical Sciences Research Council (project Atomically Deterministic Doping and Readout For Semiconductor Solotronics, EP/M009564/1). Author contributions: G.G. conceived and designed the experiments, performed the experiments, analyzed the data, and wrote the paper. A.K. performed the experiments, contributed the materials/analysis tools, and wrote the paper. T.L. contributed the materials/analysis tools. E.B. wrote the paper. H.S. wrote the paper. T.J.Z.S. contributed the materials/analysis tools and wrote the paper. G.A. conceived and designed the experiments and wrote the paper. F.K. conceived and designed the experiments and wrote the paper. N.J.C. conceived and designed the experiments and wrote the paper.

Competing interests: G.A. is a part owner and board member of the Bio Nano Consulting and an executive member of the Paul Scherrer Institut board. F.K. and E.B. do not have any direct financial interest in Keysight Technologies Inc. The other authors declare that they have no competing interests.

Data and materials availability: All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials. Additional data related to this paper may be requested from the authors. The data created during this research are openly available at https://doi.org/10.5281/zenodo.569248.

Submitted 20 October 2016 Accepted 1 May 2017 Published 28 June 2017 10.1126/sciadv.1602586

Nondestructive imaging of atomically thin nanostructures buried in silicon


Sci Adv 3 (6), e1602586.
DOI: 10.1126/sciadv.1602586