NANOTECHNOLOGY

$HfSe_2$ and $ZrSe_2$: Two-dimensional semiconductors with native high-κ oxides

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The success of silicon as a dominant semiconductor technology has been enabled by its moderate band gap (1.1 eV), permitting low-voltage operation at reduced leakage current, and the existence of SiO_2 as a high-quality "native" insulator. In contrast, other mainstream semiconductors lack stable oxides and must rely on deposited insulators, presenting numerous compatibility challenges. We demonstrate that layered two-dimensional (2D) semiconductors $HfSe_2$ and $ZrSe_2$ have band gaps of 0.9 to 1.2 eV (bulk to monolayer) and technologically desirable "high-κ" native dielectrics HfO_2 and ZrO_2, respectively. We use spectroscopic and computational studies to elucidate their electronic band structure and then fabricate air-stable transistors down to three-layer thickness with careful processing and dielectric encapsulation. Electronic measurements reveal promising performance (on/off ratio > 10^6; on current, ~30 μA/μm), with native oxides reducing the effects of interfacial traps. These are the first 2D materials to demonstrate technologically relevant properties of silicon, in addition to unique compatibility with high-κ dielectrics, and scaling benefits from their atomically thin nature.

INTRODUCTION

For over five decades, silicon has been the mainstream semiconductor for electronics due to its abundance, control of resistivity by doping, moderate band gap, and its high-quality "native" insulator, SiO_2 (*1*). In particular, the latter two properties are fundamentally responsible for enabling the efficient, low-power operation of modern silicon processors from mobile electronics to data centers. The 1.1-eV band gap is sufficiently low to allow low-voltage operation (dynamic power dissipation in logic circuits scales as the square of voltage) but sufficiently high to limit direct tunneling and leakage currents (*2*, *3*). The large, 9-eV band gap of the SiO_2 insulator and its high-quality interface with silicon are perhaps even more important in terms of enabling the isolation of silicon components and the reduction of additional gate leakage currents. This combination of properties has been difficult to replicate in other semiconductors, including Ge or compound III-V materials, despite more than half a century of research.

In the last decade, even SiO_2 has been gradually replaced in silicon electronics by the so-called "high-κ" insulators, which have higher relative dielectric constant values (κ = 16 to 20 instead of ~4 for SiO_2) and thus can be made physically thicker while maintaining the same capacitance and lower leakage (*4*, *5*). Thus, if silicon has benefited so intimately from its native SiO_2 insulator, then it is important to ask whether well-known high-κ dielectrics, such as HfO_2 or ZrO_2, are native to semiconductors which may themselves be suitable for nanoelectronics. Here, we demonstrate that layered, two-dimensional (2D) semiconductors $HfSe_2$ and $ZrSe_2$ satisfy these criteria, being compatible with desirable high-κ dielectrics and maintaining moderate band gaps in the 0.9- to 1.2-eV range down to monolayer thickness.

Two-dimensional semiconductors have attracted much attention, with subnanometer-thin single layers (1L) enabling nanoscale transistors and a lack of dangling bonds avoiding surface roughness scattering, which dominates in ultrathin silicon films (*6*–*9*). These 2D materials have nonetheless introduced new challenges, such as a larger electronic gap (of the order of 2 eV in single-layer WSe_2, MoS_2, and black phosphorus) (*10*, *11*) and non-negligible contact resistance (*8*) increasing the voltage required for device operation. Moreover, high-κ gate insulators (for example, HfO_2, ZrO_2, and Al_2O_3) cannot be easily integrated with most 2D materials because of the aforementioned chemically inert surfaces free of dangling bonds (*6*, *12*). Proposed solutions include evaporated metal-oxide buffers (*13*) and ozone or O_2 plasma treatments to create nucleation sites for further oxide growth by atomic layer deposition (ALD) (*12*, *14*–*17*). However, this interfacial engineering perpetuates a long-standing flaw in high-κ integration on silicon, wherein several angstroms of native SiO_x are grown as a buffer, deteriorating the series capacitance of the combined dielectric gate stack (*4*, *5*). In addition, for Mo- and W-based dichalcogenides, this approach is nonideal because MoO_3 and WO_3, respectively, are not good insulators and may even act as dopants (*15*, *17*, *18*).

Here, we focus on the layered diselenides $HfSe_2$ and $ZrSe_2$ (*19*–*23*), motivated by their moderate band gap (0.9 to 1.1 eV in bulk) (*22*, *24*) and their possibility of forming native HfO_2 and ZrO_2 high-κ dielectrics (*24*). This was recently observed for HfS_2, which is a material with wider bulk gap of ~2 eV (*25*, *26*). We first elucidate the electronic structure for both semiconductors, combing measurements by angle-resolved photoemission spectroscopy (ARPES) and computational projections, which reveal minimal band gap renormalization down to single layer thickness. Cross-sectional electron microscopy provides insight into the formation of the high-κ oxides, which had previously limited device studies to bulk (10 to 20 nm thick) $HfSe_2$ transistors with low current densities (*27*–*29*). We achieve air-stable devices by an entirely air-free fabrication scheme using nitrogen gloveboxes, vacuum transfer chambers, and protective encapsulation layers. Transistors down to three-layer (3L) thickness display low hysteresis, on/off current ratio of >10^6, and current density up to ~30 μA/μm. We also uncover the advantages of pairing these materials with their

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native high-κ oxides, which suppress the thermal activation of interfacial trap states.

RESULTS

Electronic band structure

We synthesized bulk crystals of $HfSe_2$ and $ZrSe_2$ from elemental precursors by chemical vapor transport (CVT) using iodine as a transport agent (see Materials and Methods) (*19*, *30*). Both compounds crystallize in the CdI_2 (1T) polytype with octahedral metal coordination, resembling the MoS_2 structure but with top and bottom rows of chalcogen atoms staggered relative to one another (Fig. 1A). Synthetic diselenide crystals have been previously characterized as n-type semiconductors, with optical absorption (*19*, *20*, *23*), ARPES (*22*), and scanning tunneling spectroscopy (STS) (*24*) measurements establishing indirect band gaps of ~1.1 to 1.2 eV for bulk $HfSe_2$ and $ZrSe_2$, respectively. The STS measurements also revealed a ~4.0-eV electron affinity χ for $HfSe_2$ (*24*), analogous to bulk Si, χ = 4.05 eV (*31*).

We performed ARPES on vacuum-cleaved, centimeter-scale crystals, initially mapping Fermi levels E_F ~ 1.0 to 1.2 eV above valence band maxima (VBM) at the central Γ point (see fig. S1), matching similar reports for molecular beam epitaxy–grown, undoped 3L-$ZrSe_2$ and six-layer (6L)–$HfSe_2$ (*32*, *33*). In situ electron doping via sodium evaporation raised E_F by ~100 meV, revealing features that correspond to conduction band minima (CBM) at the six shared *M* points of the reciprocal cell in both materials (Fig. 1, B and C). Indirect band gaps $E_{\Gamma\text{-}M} \approx 1.07$ eV (1.30 eV) were extracted for bulk $ZrSe_2$ ($HfSe_2$), slightly exceeding theoretical values of 1.02 eV (1.18 eV) from density functional theory (DFT) superimposed as lines in Fig. 1 (see section S1 for details). The hybrid density functional (HSE06) (*34*) used in the present DFT calculations correctly describes the band gap of both $ZrSe_2$ and $HfSe_2$ and agrees in fine detail with the experimental measurements, including valence sub-band structure (see further discussion in section S1, including recent underestimates of this gap by other DFT techniques). Full band structure calculations (fig. S2) project slightly smaller gaps between Γ and *L*, the cross-plane analog of the *M* point in the reciprocal lattice, representing a more 3D bulk electronic dispersion than that of Mo- or W-based 2D semiconductors (albeit one previously proposed in corrections to structural models for $ZrSe_2$) (*22*, *35*). Although not measurable in our ARPES configuration, bulk values of $E_{\Gamma\text{-}L} \approx 0.84$ eV (1.02 eV) are calculated for $ZrSe_2$ ($HfSe_2$). The latter emerges as a strong candidate for the 1.13-eV energy gap of 10L-thick $HfSe_2$ revealed by STS measurements (*24*), given the magnitude of our other underestimates. Our calculations also project minimal renormalization of electronic gap down to single layer (fig. S2), with the disappearance of interlayer *L* points and a lowering of CBM at *M* producing $E_G = E_{\Gamma\text{-}M} \approx 0.95$ eV (1L-$ZrSe_2$) and 1.13 eV (1L-$HfSe_2$).

This minor band gap renormalization relative to MoS_2 and other 2D semiconductors is partially attributed to the 1T crystal structure resulting in conduction band *L* valleys sitting energetically below those at *M* points (see fig. S2 for experimental 1T structure contrasted with fig. S3 for a hypothetical 2H structure). Sample thinning would raise the energy of *L* minima while lowering those of *M*, with the former no longer present in isolated monolayers. Moderate, indirect band gaps from ~0.9 to 1.2 eV are thus expected to persist from bulk to single layer in these selenides, which bodes well for low-voltage operation requirements in nanoscale transistors.

Ambient oxidation and air-free fabrication

To understand the process of $HfSe_2$ and $ZrSe_2$ oxidation (*24*, *27*), we turn to cross-sectional transmission electron microscopy (TEM) in Fig. 2 (see Materials and Methods). Multilayer samples were exfoliated onto Si in an inert environment [nitrogen glovebox, O_2 and H_2O < 1 parts per million (ppm)], solvent-cleaned, and left exposed to open laboratory air for variable time intervals. Figure 2A presents cross sections for a smaller $ZrSe_2$ flake (~50 nm thick, <10 μm in size) after 3 days of exposure, and Fig. 2B examines a larger, thicker (>120 nm) $HfSe_2$ flake after 7 days. High-resolution imaging of the former sample reveals growth of an amorphous oxide, primarily from the top-down but also with a smaller bottom interface component (from lateral diffusion of oxygen and moisture). Energy-dispersive x-ray (EDX) mapping of elemental lines indicates clear displacement of Se by O in structurally amorphous regions, relative to the layered bulk, whereas constant metal concentrations throughout suggest formation of sub-stoichiometric ZrO_x.

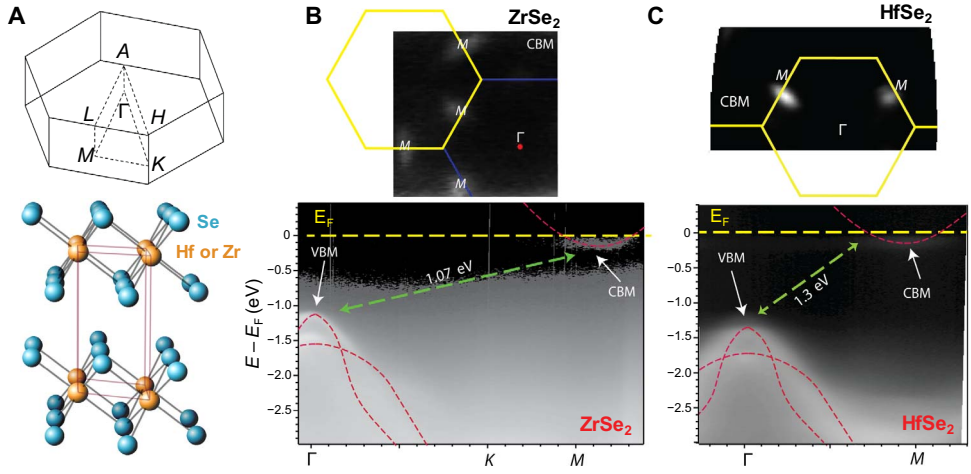

Fig. 1. Physical and electronic structure. (**A**) Crystal structure of $HfSe_2$ and $ZrSe_2$ along with reciprocal unit cell (top) outlining high-symmetry points. In-plane ARPES spectra of in situ vacuum-cleaved, Na doped (**B**) $ZrSe_2$ and (**C**) $HfSe_2$ reveal a band structure around the VBM (at Γ point) and lower edges of CBM (at *M* point), along with reciprocal space distributions of degenerate CBM valleys. Dashed red lines are the theoretical band structure from DFT calculations (HSE06 hybrid functional) in the Γ to *M* direction, adjusted for a ~0.05-eV (~0.12 eV) underestimate for Γ to *M* energy gaps of $ZrSe_2$ ($HfSe_2$).

For the larger $HfSe_2$ sample in Fig. 2B, a pristine bottom interface is obtained against a thin buffer of native SiO_2, despite longer exposure times producing a thicker amorphous HfO_x top film. These experiments suggest that ambient oxidation is not self-limiting for our layered selenides, ostensibly aided by oxygen diffusion through atomic-scale imperfections, such as Se vacancies. Simultaneous top and bottom growth of amorphous metal oxides is comparable to that observed in few-layer metallic 1T-TaS_2 by analogous FIB (focused ion beam) and TEM imaging (*36*). We estimate initial ambient oxidation rates of 5 to 10 nm per day for our large-area, bulk samples, depending on the degree of volumetric expansion during this process (*25*), and gradually declining over time as access is restricted to buried layers. Oxidation rates may increase from lateral diffusion of oxygen and moisture on smaller, few-layer samples and are further accelerated by open-air processing and any heating. These technologically relevant oxides present novel opportunities for high-κ dielectric integration, as readily observed by laser heating oxidation of $ZrSe_2$ crystals directly into tetragonal and monoclinic ZrO_2 (fig. S4).

Figure 3A shows the schematic of a completed few-layer $HfSe_2$ or $ZrSe_2$ transistor. To limit the ambient oxidation of these materials and obtain stable few-layer devices, we developed a completely air-free fabrication scheme in which material surfaces are exposed only to inert atmospheres (multiple nitrogen gloveboxes, O_2 and H_2O < 3 ppm) or vacuum chambers throughout processing. In situ glovebox capabilities included electron beam (e-beam) resist spinning/baking and ALD of multiple dielectrics, facilitating protective encapsulation before transfer to external lithography and probing tools (see Materials and Methods). $HfSe_2$ and $ZrSe_2$ flakes were exfoliated onto 90-nm SiO_2 on p^+ Si substrates in a N_2 atmosphere and immediately capped with a 25 Å film of amorphous AlO_x by low-temperature ALD [alternating trimethylaluminium (TMA) and H_2O pulses at 150°C] loaded directly from the glovebox. This thin dielectric plays a dual role, both as a protective encapsulation layer against trace oxygen or moisture (as recently applied for air-stable capping of WTe_2) (*37*) and as a thin tunnel barrier for charge injection in metal-interlayer-semiconductor (MIS) contacts (Fig. 3A). MIS contacts use an ultrathin interlayer to separate metals from semiconductors, preventing Fermi level pinning in the semiconductor band gap (*38*). The 25 Å AlO_x barrier provided optimum yield of transistors, and comparable MIS layers have led to improvements in contact resistance R_C for MoS_2 with Al-, Ta-, and Ti-metal oxides (*39*, *40*).

These capped flakes were coated with 300-nm poly(methyl methacrylate) (PMMA; N_2 atmosphere), providing temporary encapsulation while serving as e-beam resist for local marker and contact patterning. Resist development was followed by vacuum chamber transfer into a metal evaporator (see Materials and Methods), depositing Cr/Au contacts (15/45 nm). Ti/Au, Pd, Ag, and pure Au contacts were also evaluated, spanning a work function range of ~1 eV, but achieved significantly worse n-type performance. After metal lift-off in the original glovebox, the interfaced ALD chamber was used to enclose devices within a further 200 Å of AlO_x, serving as an oxygen and moisture barrier during transfer to a vacuum probe station in which a final 1-hour 250°C anneal was performed.

Compatibility of exfoliated samples with high-κ dielectrics was evidenced by the uniform nucleation of AlO_x capping layers, which were free of pinholes and of equivalent roughness (root mean square, ~0.35 nm) both on and off flake surfaces under atomic force microscopy (AFM) topographic mapping. Smooth oxide coverage enabled direct layer counting from AFM height profiles, correlating flake thickness to approximate integer multiples of the interlayer spacing of $HfSe_2$ and $ZrSe_2$ (both ~0.62 nm) (*19*, *20*).

Figure 3B shows a cross-sectional TEM image from the channel of an eight-layer (8L) $HfSe_2$ device (confirming its AFM thickness) with outlines of the first seven layers clearly visible and partial signs of an eighth layer blending into the top AlO_x film. Its consumption by the top dielectric suggests partial oxidation during fabrication, despite extensive efforts to limit trace oxygen and moisture, carefully seeding ALD at reduced temperatures (see Materials and Methods). TEM cross sections at device contacts (fig. S6) show similar features, with discernable outlines of a broadened top layer contributing up to ~5 Å to the ~25 Å MIS oxide (consistent with reports of 250% cross-plane volumetric expansion in oxidized HfS_2, as well as increased thickness for O_2 plasma–exposed $HfSe_2$) (*25*, *29*). TEM profiles qualitatively resemble those of HfO_x on partially oxidized WSe_2 top layers, following "self-cleaning" ALD reactions reducing a surface WO_x layer formed by ozone exposure (*16*). However, a fortuitous native HfO_x layer presents clear benefits for gate integration compared to trace metallic W or Mo (or their conductive oxides in the absence of self-cleaning reduction).

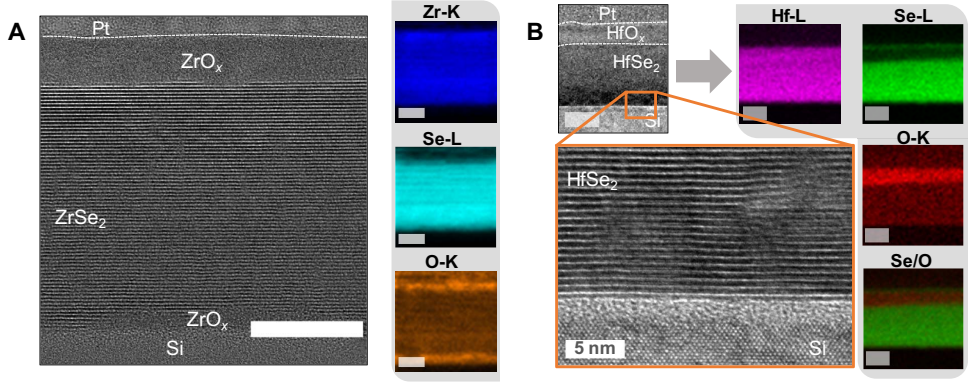

Fig. 2. Cross-sectional TEM and EDX mapping of native oxide formation. (**A**) Cross-sectional TEM image of a smaller (<50 nm thick, <10 μm in lateral size) $ZrSe_2$ flake following 3 days of ambient exposure, demonstrating both top-down and bottom-up oxidation into amorphous ZrO_x, which partially consumes individual layers. Insets show that EDX elemental mapping demonstrates displacement of Se by O in oxidized regions. Scale bars, 20 nm. (**B**) Similar TEM images of a larger (>100 μm), thicker $HfSe_2$ flake after 7 days of ambient exposure, with greater extent of top-down oxidation into HfO_x, despite a pristine bottom interface with the Si substrate. Insets show EDX elemental mapping confirming complete chalcogen depletion, illustrated via overlay of O and Se signals. Scale bars, 50 nm.

This incidental oxidation may explain the lack of measurable charge transport in samples thinner than 3L (~1.8 nm), alongside strong reduction of optical contrast for bilayer flakes, suggesting complete consumption. The proximity of an oxidized layer to a 2D electron gas (2DEG) holds several implications to subsequent discussions of trap states and interfacial engineering. Samples are hereafter referred to by AFM-assigned layer counts (for example, 3L or 8L), although it is likely that the topmost layer(s) do not contribute to charge transport because of partial oxidation.

Encapsulated device characterization

Figure 3 (C and D) shows current versus gate voltage (I_D versus V_{GS}) measurements of few-layer $HfSe_2$ transistors, modulated using the back gate shown in Fig. 3A. Samples between 3 and 13 layers thick (~1.8 to 8.1 nm) were probed under vacuum, with channel length varying from L = 90 nm to L = 2.5 μm. Devices of all thicknesses demonstrated clear turn-off, with on/off current ratios of ~10^6 at 300 K for source-drain bias V_{DS} = 1 V (approaching 10^7 for thicker samples cooled to 200 K). As marked by the arrows, all data shown are double sweeps around back-gate V_{GS} = 0 V, revealing relatively low hysteresis consistent with previous reports for vacuum-annealed 2D transistors under AlO_x encapsulation (*41*). Current densities of shortest devices (90 to 150 nm) reached 25 to 30 μA/μm (Fig. 3C, inset), although superlinear dependence on V_{DS} suggests contact-limited behavior. These current densities represent two orders of magnitude improvement over previous reports in substantially thicker HfS_2 and $HfSe_2$ devices at comparable biasing (*25*, *27*–*29*). Inverse subthreshold slope (SS) of 3.2 to 4.2 V per decade is found on the 90-nm SiO_2 back-gate oxide, although SS is likely limited by the relatively thick tunnel barriers at our unoptimized MIS contacts. Similar SS values were reported for few-layer MoS_2 on comparable back gates, with larger Schottky barriers to the conduction band (*42*).

Room temperature field-effect electron mobilities μ_{FE} = 1 to 4 $cm^2 V^{-1} s^{-1}$ (Fig. 3D, inset) are extracted as $\mu_{FE} = L/(C_{ox} V_{DS} W)(dI_D/dV_{GS})$, where W is the channel width and $C_{ox} \approx 38$ nF/cm^2 is the capacitance of the SiO_2. Mobility values are modestly improved (by a factor of ~2 to 5×) when accounting for contact resistance via transfer length measurement (TLM) analysis on devices with multiple channel lengths (fig. S7), revealing non-negligible $R_C \approx$ 50 to 100 kilohms·μm. This contact resistance is two orders of magnitude greater than that of the best MoS_2 devices (*8*) but is not unexpected for the unoptimized MIS contacts used here, with possible material degradation at exposed contact regions during partial vacuum transfer to an external metallization tool. We note that the mobility estimate is complicated here by temperature-dependent shifts of the threshold voltage, as described below. Chemical stability of the alumina capping layer resulted in minute (few percentages) degradation of device currents after 1 to 2 months of storage in nitrogen ambient, with comparably stable hysteresis and threshold voltage. Open-air aging of devices (fig. S5) indicates that this encapsulation provides several weeks of ambient stability.

Figure 4 shows qualitatively similar trends for AlO_x-capped $ZrSe_2$ devices with identical MIS contacts, albeit with lower mobilities (relative to our $HfSe_2$) despite smaller projected semiconducting band gaps, E_G = 0.84 eV. Air-stable encapsulation of films from 3L to bulk enabled Raman spectroscopy of characteristic phonon modes (Fig. 4A), comparable to reported values of cross-plane A_{1g} (193 cm^{-1}) and in-plane E_g (145 cm^{-1}) peaks (*43*). These modes shift very little (<1 cm^{-1}) as film thickness is reduced compared to other dichalcogenide crystals (*6*). Transistor transfer curves show current densities approaching 20 μA/μm (Fig. 4B) and on/off ratios of 10^5 to 10^6 for 5L- to 6L-thick devices with submicrometer channel lengths (Fig. 4C), achieving room temperature μ_{FE} = 1 to 1.5 $cm^2 V^{-1} s^{-1}$. The thinnest working devices were again 3L, although these demonstrated reduced drive currents ($I_D \approx$ 0.1 μA/μm and $I_{ON}/I_{OFF} \approx 10^5$ for L = 0.52 μm) and contact-limited mobility (0.1 $cm^2 V^{-1} s^{-1}$) relative to channels thicker than 5L. Sensitivity to material degradation may be more acute for $ZrSe_2$, although no outward signs of oxidation or poor dielectric coverage were found in scanning electron microscopy (SEM) analysis (Fig. 4, C and D, insets). Cooling to 80 K revealed improved on/off current ratios across all devices, to ~10^7 for the 6L sample in Fig. 4D, alongside forward shifts in threshold voltage V_T resembling those of AlO_x-capped $HfSe_2$ devices in Fig. 3D. Subthreshold swing nearly halves from 3.5 V per decade at room temperature to 1.5 to 2 V per decade below 150 K.

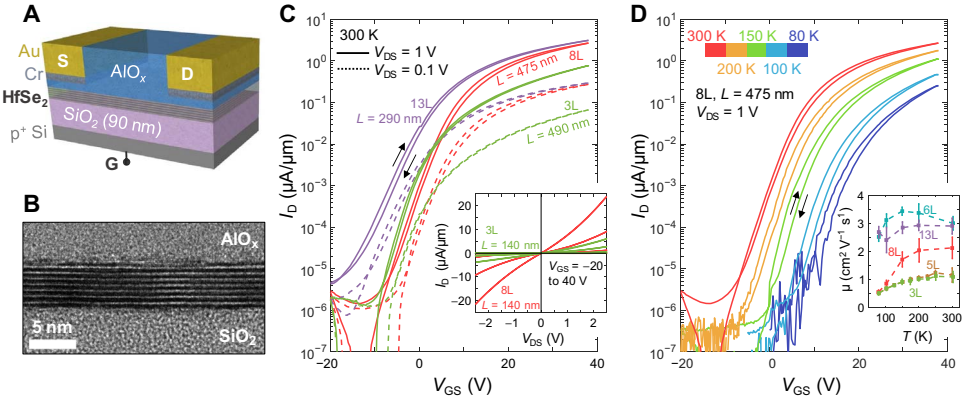

Fig. 3. $HfSe_2$ transistors. (**A**) Schematic of $HfSe_2$ device, back-gated through 90-nm SiO_2, and with ALD alumina used as both protective encapsulation and a ~25 Å interlayer in an MIS contact scheme (contact layers not to scale; capping alumina over contact metals not shown). (**B**) High-resolution TEM image of the channel of an 8L-thick $HfSe_2$ device, with evidence of a partially oxidized top layer integrated into the capping oxide. (**C**) Room temperature transfer curves of $HfSe_2$ transistors with varying channel thickness, demonstrating an on/off current ratio of ~10^6 at V_{DS} = 1 V. Inset: Linear I_D versus V_{DS} plots for short-channel devices ($L \approx$ 140 nm) with 3L and 8L channels. All curves are dual sweeps from the origin, demonstrating low hysteresis (see arrows). (**D**) Temperature dependence of transfer curves for the 8L-thick $HfSe_2$ device, from 80 to 300 K. The threshold voltage shifts higher as the sample is cooled. Inset: Field-effect mobilities of encapsulated 3L to 13L (~1.8 to 8.1 nm thick) $HfSe_2$ devices.

Understanding the interfaces

The negative shift of threshold voltage observed with increasing temperatures (Figs. 3D and 4D) has precedent in 2D electron systems; it has been examined in heterostructure field-effect transistors [HFETs; alternatively labeled high–electron mobility transistors (HEMTs)] formed by confined 2DEGs near conduction band offsets at junctions such as AlGaN/GaN (*44*–*46*). This phenomenon is particularly prominent in AlGaN/GaN and InAlN/GaN devices with Al_2O_3 top-gate dielectrics, where it was attributed to thermal activation of charge traps at defect sites in imperfect semiconductor-oxide interfaces (*45*, *46*). Negative V_T shifts with elevated temperature are triggered by donor states deep (~200 meV) within the band gap, contributing free carriers despite a spatial offset of several nanometers between the oxide interface and the buried 2DEG. This is facilitated by the polarity of the channel material, a common property of III-V compounds and of layered Hf- and Zr-based dichalcogenides (*6*, *21*).

The interface of our oxidized top channel layer appears to play a similar role to the oxide-nitride cap interface in HEMTs. Our MIS contact scheme allows substitution of different thin "I" layers while retaining air-stable encapsulation with a global 20-nm alumina. We evaluated two configurations across multiple $HfSe_2$ devices 3L to 8L thick, using 25 Å layers of AlO_x and HfO_x (Fig. 5A) deposited immediately after exfoliation in a glovebox ALD system at 150°C. For AlO_x interlayers, the general trends of Figs. 3D and 4D are replicated in back-gate sweeps across all channel thicknesses; average threshold voltage shifts ΔV_T of 10 to 15 V are recorded while cooling from 300 to 80 K in Fig. 5B (blue data points).

This consistent temperature dependence of V_T enables estimates of trap density N_{IT} from a simplified HFET charge-neutrality model (*45*), $N_{IT} = \Delta V_T(2C/q)$. Here, C is the net capacitance per area, calculated from the series combination of C_{ox} and a finite semiconductor depth (C_s with $\kappa_{HfSe2} = 8.05$) (*47*), assuming a 2DEG peaked at the center of flake thickness (*48*). Despite a lower gate capacitance than that of conventional HFETs, dominated by the single back gate across all sample thicknesses, a range of $N_{IT} = 3 \times 10^{12}$ to 8×10^{12} cm^{-2} for the $HfSe_2/HfO_x/AlO_x$ stack mirrors the 2.5×10^{12} to 7.5×10^{12} cm^{-2} estimated for MoS_2/AlO_x top-gate interfaces via hysteresis, SS, and charge collection spectroscopy (*49*, *50*). Figure 5C shows an Arrhenius analysis of the trap thermal response, fitting an exponential evolution of density N_{IT} with temperature by an activation energy $E_A \approx 26$ to 32 meV comparable to the Boltzmann energy at room temperature. The characteristic shift in transfer curves for AlO_x interlayers is thus associated with a high density of relatively shallow trap states, which activate on an energy scale corresponding to heating from 80 K to ambient.

Devices with HfO_x MIS contacts (orange data points in Fig. 5B) have smaller threshold shifts down to 80 K, lacking the monotonic increase seen in all AlO_x samples. This can also be seen by comparing the inset of Fig. 5B (hafnia interface to $HfSe_2$) with Figs. 3D and 4D (alumina interface). In other words, the transfer curves at 80 and 300 K are nearly the same, except for the sharper turn-on at the lower temperature. Device on/off ratio, subthreshold swing, and mobility remain similar to those with all AlO_x encapsulation (Fig. 3), despite slight widening of the hysteresis envelope (from ~1 to ~2 V across a 60 V sweep). The choice of an HfO_x interlayer, nominally the native oxide of the constituent transition metal, thus offers measurable improvement of the interfacial quality. Further studies are needed to develop a mechanistic understanding of this phenomenon, that is, whether it is grounded in a fundamental material compatibility between ALD oxides and self-limiting, oxidized diselenide layers, or it is a consequence of the difference in material dielectric constant ($\kappa_{HfOx} \approx 2\kappa_{AlOx}$). Regarding the former hypothesis, the oxidized top $HfSe_2$ layer may be best passivated by ALD of the same metal oxide, potentially driving more complete oxidation of this layer. Less reactive AlO_x growth may produce an inconsistent $AlO_x/HfSe_{2-y}O_y$ interface, containing the traps quantified in Fig. 5C.

Top-gated transistors with native high-κ oxides

To exploit the native integration of HfO_2 with $HfSe_2$, we fabricated the first top-gated transistors of this kind, as shown in Fig. 6. These devices include the 2.5-nm MIS contacts discussed earlier and a further 17-nm layer of HfO_2 deposited by ALD [with a total equivalent oxide thickness (EOT) ≈ 4.75 nm]. A Cr/Ag metal gate is patterned by a negative-tone resist process, protecting channel regions by low-energy metal deposition and no direct exposure to e-beam patterning (see Materials and Methods). Figure 6 shows the current versus top-gate voltage of such a transistor with 7L channel thickness and ~1 μm channel length (the gate length is slightly larger, overlapping the contacts). DC sweeps

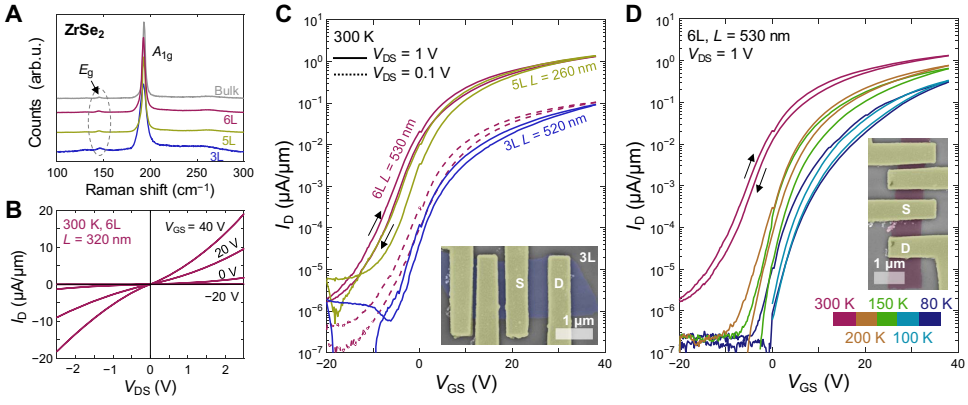

Fig. 4. $ZrSe_2$ transistors. (**A**) Low-power Raman spectra of $ZrSe_2$ devices encapsulated by AlO_x, from 3L to bulk, with minute shifts of A_{1g} (~193 cm^{-1}) and E_g (~145 cm^{-1}) modes as the thickness is reduced (532 nm laser). arb.u., arbitrary units. (**B**) Hysteresis-free room temperature I_D versus V_{DS} forward and reverse sweeps for a 6L-thick $ZrSe_2$ transistor (L = 320 nm) with a current density up to ~20 μA/μm. (**C**) Transfer curves of back-gated $ZrSe_2$ transistors of varying channel thickness show lower current density in the thinnest (3L) devices. (**D**) Temperature-dependent transfer curves of the 6L device between 80 and 300 K show improved on/off current ratios with cooling (approaching 10^7) and forward shift in threshold voltage at lower temperatures. Insets are false-colored SEM micrographs of 3L and 6L devices, with source (S) and drain (D) contacts as labeled.

starting at V_{GS} = 0 (solid black curve) manifest current modulation up to 10^6, with hysteresis and nonideal SS (200 to 350 mV per decade) indicative of charge trapping (*49*).

Nonetheless, most charge trapping effects can be bypassed with pulsed measurements (red dashed lines in Fig. 6) using pulse widths shorter than average charge trapping time constants. Using 125 μs wide V_{GS} pulses with 10 μs rise and fall time drastically reduces the hysteresis and enhances current density to values comparable with our previous back-gated transistors. The contact-limited field-effect mobility is ~0.3 $cm^2\ V^{-1}\ s^{-1}$, lower than in back-gated devices ostensibly because of scattering at the top interface with the partially oxidized layer and lack of gating under contact regions. We note that top-gated transistors are more sensitive to interfacial traps than back-gated devices, given that current flow is concentrated at the top $HfSe_2$ interface (versus the middle or bottom interface in back-gated devices) (*48*). These results further emphasize the continued need to study high-quality native oxide formation in these top-gated transistors.

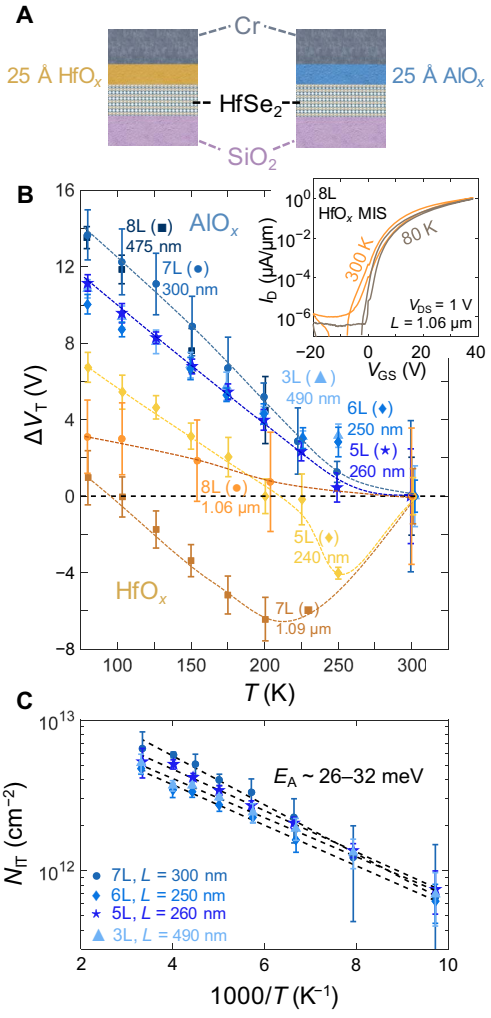

Fig. 5. Interfacial oxide engineering. (**A**) Configuration of MIS contacts for $HfSe_2$ transistors with 25 Å interlayers of either AlO_x or HfO_x ALD oxide (global 200 Å alumina capping is used for both). (**B**) Mean shift in threshold voltage ΔV_T from the 300 K baseline for multiple $HfSe_2$ devices cooled to ~80 K, contrasting the effects of AlO_x (blue) and HfO_x (orange) interlayers. V_T was extracted from the linear intercept at the point of peak transconductance. Dashed lines are guides to the eye. Inset shows transfer characteristics of an 8L-thick $HfSe_2$ device with HfO_x interlayer at 80 and 300 K, demonstrating a minimal shift of V_T and steeper turn-on behavior at lower temperatures. (**C**) Temperature evolution of estimated interfacial trap density N_{IT} for multiple $HfSe_2$ devices with AlO_x interlayers, as calculated from ΔV_T (see text). Dashed lines are fits to Arrhenius activation energies of 26 to 32 meV.

DISCUSSION

Several discoveries made in the course of this work suggest advantages of both $HfSe_2$ and $ZrSe_2$ for 2D electronics. First, unlike MoS_2 or black phosphorus, the band gap of these selenides appears to change very little as the material thickness is scaled from bulk to single layers, remaining indirect and in the 0.9- to 1.2-eV range. This invariance is likely to enable higher tolerance for variability in system-level applications because large-area growths could yield a combination of single- and few-layer regions (*6*). Second, the band gap is comparable to that of silicon, small enough to allow low-voltage operation of future electronics but large enough to enable >10^6 on/off current ratios, along with the benefits of 2D materials (namely, an atomically thin body for ultrascaled transistors). In contrast, most other 2D semiconductors have larger band gaps around 2 eV or higher in single layers.

Third, $HfSe_2$ and $ZrSe_2$ benefit from native oxides HfO_2 and ZrO_2, a property similar to that of silicon, but with technologically more desirable high-κ insulators. This behavior is rare among known semiconductors because desirable oxides form neither on Ge and III-V compounds, nor on other moderate-gap 2D semiconductors. Thus, results shown here represent the first demonstration of 2D transistors with native high-κ oxides, although further work is needed to improve the quality of the interfaces obtained. A fourth advance made in this work is the air-free processing of these materials with standard microfabrication techniques, which has enabled our study of thinner samples (down to 3L) with higher current densities (up to ~30 μA/μm) than has been achieved even on bulk samples with these materials.

Transistor performance may be improved with refined processing, engineering contacts and interfaces toward enhanced current densities and intrinsic mobility. We note that, even in air-stable MoS_2, existing measurements record several orders of magnitude variation in these parameters, depending on contact and channel processing, as well as top/bottom interfaces (including mitigating effects of substrate roughness, adsorbates, and charge traps by encapsulation in insulating van der Waals heterostructures) (*51*, *52*). Across our yet unoptimized devices, imperfect MIS contacts with relatively thick "I" barriers could be avoided by development and metallization in an entirely enclosed, inert atmosphere. Threshold voltage shifts also appear to be induced by shallow interfacial trap states, highlighting novel challenges of interfacial engineering for layered materials with native oxides formed during processing. Selective oxidation of only the topmost layer(s) would enable improved growth of desirable high-κ dielectrics, for example, by controlled, layer-selective oxidation with pulsed ozone or oxygen plasma recently applied to other 2D materials (*12*, *15*, *17*).

CONCLUSIONS

In summary, we performed a systematic evaluation of $HfSe_2$ and $ZrSe_2$, layered 2D materials with native high-κ dielectrics, demonstrating the first such electronic devices with few-layer channels. Computational and ARPES studies reveal minimal change of electronic band gap with decreasing layer number, whereas TEM characterization identified the formation of amorphous native oxides. Stable devices, fabricated under

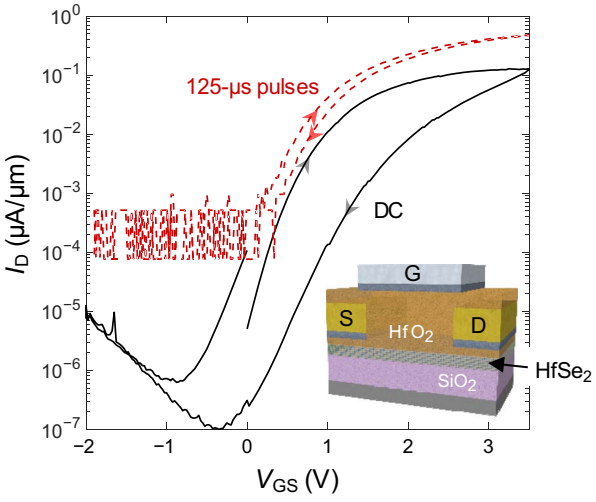

Fig. 6. Top-gated $HfSe_2$ transistor with native HfO_2 dielectric. Measured transfer characteristics of a top-gated 7L-thick $HfSe_2$ transistor with 2.5-nm HfO_x MIS contacts and 19.5-nm HfO_2 top-gated dielectric (EOT ≈ 4.75 nm). The channel length is $L \approx 1$ μm, $V_{DS} = 1$ V, and $T = 295$ K, and the Si substrate was grounded. DC measurements (solid black lines) reveal ~10^6 on/off current ratio, despite noticeable hysteresis and SS of ~200 to 350 mV per decade. Pulsed measurements (dashed red lines, with 125 μs pulse width and 10 μs fall/rise times) reduce the hysteresis and achieve higher current density, although the low-current resolution is limited. Inset shows device schematic with source (S), drain (D), and gate (G) electrodes as labeled.

inert atmospheres, demonstrated multiple orders of magnitude improvement in current density for these materials relative to bulk studies (*27*–*29*). We also conducted a preliminary study of interfacial trap states and their suppression through the choice of compatible dielectrics. Both $HfSe_2$ and $ZrSe_2$ have moderate band gaps, regardless of layer number, and readily form native high-κ oxides, reproducing for the first time two key attributes of silicon for large-scale technological integration in a 2D nanomaterial, intrinsically scalable to the atomically thin limit.

MATERIALS AND METHODS

Crystal growth

Bulk crystals of $HfSe_2$ and $ZrSe_2$ were grown by CVT from stoichiometric mixtures of elemental Hf powder (Alfa Aesar, 99.6%), Zr slugs (Alfa Aesar, 99.95%), and Se powder (Alfa Aesar, 99.999%). These were sealed in quartz tubes evacuated under argon, with iodine (Alfa Aesar, 99.99+%) added at 5 mg/cm^3 as a transport agent. Growth took place for 14 days along an 11-cm transport length, corresponding to a ~100°C thermal gradient in a single-zone furnace with central temperatures of 900° or 950°C. Both temperatures produced large amounts of platelet-like crystals with facets several millimeters to >1 cm in size. $ZrSe_2$ crystals were uniformly dark green, whereas those of $HfSe_2$ were metallic gray.

ARPES measurements

ARPES measurements were performed at Beamline 10.0.1.1 of the Advanced Light Source of Lawrence Berkeley National Laboratory. Bulk crystals were cleaved in situ at 10 K in ultrahigh vacuum. Sodium was evaporated onto the cleaved sample surface in situ, with pressure less than 10^{-10} torr during evaporation. All data were collected using 75 eV photons. ARPES measurements were carried out with a total energy resolution of ~25 meV and base pressures below 5×10^{-11} torr.

DFT calculations

DFT calculations were performed using the hybrid density functional HSE06, as implemented in the Vienna Ab initio simulation package (*34*). In the HSE06 functional, 25% of the short-range exchange interaction of the Perdew-Burke-Ernzerhof generalized gradient approximation was replaced by the short-range nonlocal Hartree-Fock exchange interaction (*34*). For this study, an exchange-screening parameter ω of 0.2 Å^{-1} was applied for both $HfSe_2$ and $ZrSe_2$. All calculations were performed using the projector augmented wave method; Zr (4s, 4p, 5s, and 4d), Hf (5p, 6s, and 5d), and Se (4s and 4p) were used as valence electron states, and spin-orbit coupling was included in the calculations. Bulk (8 × 8 × 8) and monolayer (8 × 8 × 1) Γ-centered *k*-point grids were used, with structures optimized for lattice constants and internal ionic coordinates until the residual forces were less than 0.01 eV/Å.

Device fabrication and characterization

Flakes of Hf/$ZrSe_2$ were exfoliated onto 90-nm SiO_2 on p^+ Si substrates in a nitrogen atmosphere (glovebox; O_2 and H_2O < 3 ppm) using a low-residue thermal release tape (Nitto-Denko Revalpha) and cleaned with an acetone/2-propanol soak. AlO_x or HfO_x (25 Å) interlayers were deposited in situ within an interfaced Cambridge Savannah Thermal ALD chamber [150°C, alternating H_2O and TMA or tetrakis(dimethylamido)hafnium pulses, after first saturating surfaces with 10 pulses of metal precursor], followed by spin coating of 300 nm PMMA e-beam resist (Microchem A5 950k). Samples were briefly removed from gloveboxes for mapping of target flakes and e-beam lithography of contacts (Raith 150, 20 kV), retaining PMMA coverage throughout. Patterned samples were developed in a N_2 glovebox and loaded into a custom, closed transfer stage that was pumped to ~2×10^{-5} torr and mounted inside a Lesker PVD 75 e-beam evaporator. Once mounted, this stage could be manually actuated to open when external chamber pressure matched that inside, thereby limiting contact of exposed flake surfaces to trace oxygen or moisture. Cr/Au (15/45 nm) contacts were deposited at base pressures of ~5×10^{-8} torr, with lift-off performed using acetone/2-propanol in the original glovebox. A further 200 Å AlO_x capping layer was deposited (ALD, 150°C; TMA/H_2O) before transfer to a Janis Cryogenic vacuum probe station (chamber pressure, 10^{-6} to 5×10^{-5} torr) for a final vacuum anneal (1 hour at 250°C, cooling to room temperature over several hours). Top-gated devices were fabricated in a variation of this process, depositing a 2.5-nm HfO_x interlayer and Cr/Au (15/35 nm) contacts before encapsulation with a further 17-nm HfO_x. MaN-2403 negative-tone resist (300 nm) was spun and patterned (Raith 150, 10 kV), lifting off a Cr/Ag (5/20 nm) top-gate electrode.

Electrical characterization of devices was performed in a Janis Cryogenic probe station, cooled with closed-loop liquid nitrogen, using 4225-RPM Remote Amplifier/Switch units connected to a Keithley 4200-SCS parameter analyzer. ALD-encapsulated flakes were profiled via AFM (Veeco Dimension 3100, soft-tapping mode) and Raman spectroscopy (HORIBA LabRAM, 532 nm laser source), with devices imaged by SEM (Raith 150, 5 to 10 kV). Cross sections of oxidized flakes (Fig. 2) were prepared with a FEI Helios NanoLab 600i DualBeam FIB/SEM using a lift-out method. A platinum layer was deposited onto the sample area for protection, with gallium ion milling performed right before TEM characterization. High-resolution TEM images were obtained using an aberration-corrected FEI Titan at 300 kV, with in situ EDX elemental mapping. Device cross sections (Fig. 3B and fig. S6) were prepared and imaged by Evans Analytical Group using a FEI Dual Beam FIB/SEM and FEI Tecnai TF-20 FEG/TEM at 200 kV.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/8/e1700481/DC1

section S1. Electronic band structure validation
section S2. Native oxide formation and passivation
section S3. Contact characterization
fig. S1. Undoped ARPES spectra of bulk crystals.
fig. S2. HSE06 DFT of monolayer and bulk band structure.
fig. S3. Gap divergence in hypothetical 2H-$HfSe_2$.
fig. S4. $ZrSe_2$ Raman laser oxidation.
fig. S5. Aging of capped $ZrSe_2$.
fig. S6. MIS contact TEM.
fig. S7. Contact TLM analysis.
table S1. Laser oxidation peaks.
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