NANOMATERIALS

Selective control of electron and hole tunneling in 2D assembly

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Recent discoveries in the field of two-dimensional (2D) materials have led to the demonstration of exotic devices. Although they have new potential applications in electronics, thermally activated transport over a metal/semiconductor barrier sets physical subthermionic limitations. The challenge of realizing an innovative transistor geometry that exploits this concern remains. A new class of 2D assembly (namely, "carristor") with a configuration similar to the metal-insulator-semiconductor structure is introduced in this work. Superior functionalities, such as a current rectification ratio of up to 400,000 and a switching ratio of higher than 10^6 at room temperature, are realized by quantum-mechanical tunneling of majority and minority carriers across the barrier. These carristors have a potential application as the fundamental building block of low–power consumption electronics.

INTRODUCTION

Performance improvements have led state-of-the-art silicon-based electronics to face challenges in continuing to fulfill Moore's law as a result of leakage current and electrostatic degradation (*1*). Fortunately, these challenges are expected to be met by an abundance of atomically thin, two-dimensional (2D) materials (*2*–*4*). Considering the natural advantages of 2D materials (*3*, *4*), new transistor architectures could be realized by assembling diverse van der Waals materials into a 3D structure with superior performance in terms of the on/off ratio and the subthreshold swing. A popular van der Waals heterojunction, graphene/transition metal dichalcogenides (TMDs) (*5*–*10*), mimics a graphene barristor developed and named by Yang *et al.* (*11*) and has displayed Schottky-limited transport, revealing current on/off ratio values ranging widely from 10 to 10^6 under the modulation of the Schottky barrier height ϕ_B (*5*–*7*, *9*, *10*). However, these devices have a critical weakness in the thickness of the active layer [TMDs or hexagonal boron nitride (hBN)], which exhibits either a strong temperature dependence or an unacceptably small switching ratio. The off-state current I_{off} is especially pronounced and is conceptually comparable to that of the conventional field-effect transistor (FET) (*5*, *6*, *8*, *11*, *12*) because it eventually results in either direct tunneling transport in thin devices (similar to channel shrinkage in FETs) (*9*, *10*, *13*) or thermionic emission transport with a thick active layer (long channel) by majority carriers (which are electrons in most devices) (*7*, *8*, *11*). Therefore, the challenge is to create and characterize a device that simultaneously has pure quantum tunneling transport in both the on and off states, a weak temperature dependence, and fast switching.

As a promising approach for achieving these goals, a metal-insulator-semiconductor (MIS) capacitor-like device is developed by sandwiching an insulating hBN tunnel barrier between a multilayer graphene (MGr) and an n-type tungsten disulfide (WS_2) nanosheet. Device operation relies on the tunability of the surface potential ϕ_s of WS_2 at the atomically abrupt interface that is switchable between the inversion of holes and accumulation of electrons, as controlled by the tunneling process across the insulator (Fig. 1A). Thus, a high current on/off ratio is robust for the controllability of ϕ_s by means of a Fermi level shift ΔE_{FG} in the electrostatically gated MGr. To date, a triode device based on band-to-band tunneling currents via the transition from minority to majority carriers has not been achieved; thus, we refer to our device as a "carristor" to reflect the carrier-controlled nature of the device. We have demonstrated that the proposed carristor (denoted below by MIS-C) can be created when the hBN thickness is intentionally reduced for operations away from thermodynamic equilibrium (Fig. 1B and fig. S1). In the overall study, we also fabricated alternative devices (barristors) composed of MGr-TMDs (denoted by GW-B and GM-B for WS_2 and MoS_2 active layers, respectively) for systematic comparison.

RESULTS

Figure 1C shows an optical image of one of the investigated carristors fabricated on a thermally oxidized 280-nm-thick layer of SiO_2 on a Si substrate (fig. S2). Briefly, a vertically assembled MGr-hBN-WS_2 stack was generated by the dry transfer of exfoliated nanosheets from individual bulk crystals and sandwiched by electrodes, namely, top (T1 to T3) and bottom (B) leads, to establish electrical interconnections. The details of the tunneling device fabrication procedure and the material characterization are presented in Materials and Methods. High-resolution transmission electron microscopy (TEM) allows us to verify the atomic sharpness of the interface (Fig. 1D), with a thin uniform tunnel layer of approximately 3 nm appearing both in the magnified TEM image and in the statistical histogram (for hBN/SiO_2 steps) acquired from atomic force microscopy (AFM) (Fig. 1, E and F). To construct the band lineup in the heterostructures, a conventional x-ray photoelectron spectroscopy (XPS) technique was used, which reveals a straddling heterojunction (Fig. 1G and fig. S4). When performing electrical transport measurements, the degenerately doped n^+-type silicon acted as a back gate for the modulation of V_G, and a dc bias voltage V_{TB} was applied to one of the top leads while measuring the vertical tunnel current flow I_{TB} (B is ground).

Carrier transport through the MIS system is often regarded as a leakage current in FETs (*1*, *14*, *15*). However, Fig. 2A shows that such a current becomes useful when a V_{TB} value between −3 and 3 V is applied. The output curve reveals strong asymmetric behavior that has characteristics analogous to that of a p-n junction diode or a typical Schottky diode. Therefore, the Shockley diode equation $I_{TB}(V_{TB}) = I_0[\exp(eV_{TB}/\eta k_B T) - 1]$ can be used for quantitative characterization, where I_0, e, η, k_B, and T are the saturation current, the elementary

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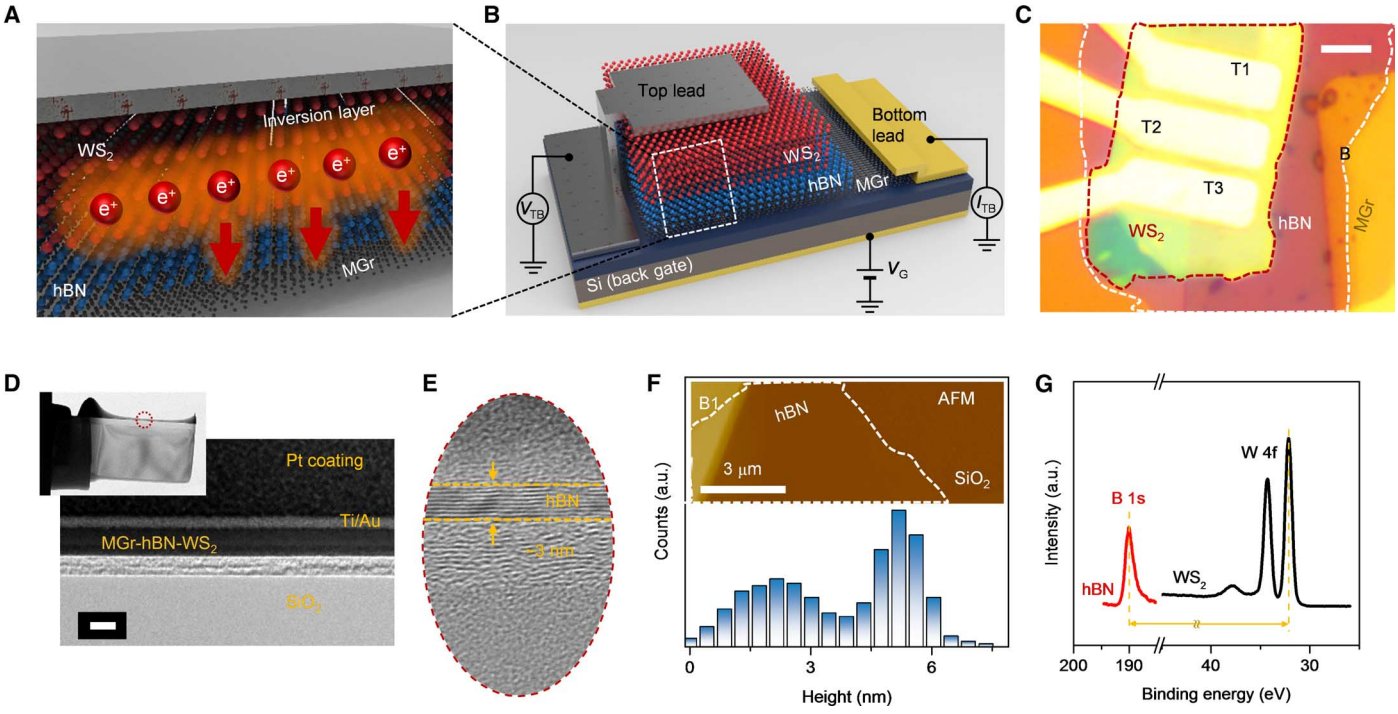

Fig. 1. Illustration of MIS-C and the characterization of the device structure. (**A**) Schematic illustration of an MIS-C under the state of forming an inversion of holes for tunneling. "e^{+}" represents the hole carrier. (**B**) Schematic representation of the carristor layout and electrical connections for electrical transport measurements. (**C**) Optical image of a typical MIS-C with Ti/Au top and bottom contacts. Scale bar, 5 μm. (**D**) High-resolution TEM image of an MGr-hBN-WS_2 heterostructure fabricated on a SiO_2/Si substrate with a titanium metal capping layer (corresponding to the top lead). The layer thicknesses of the MIS-C are 10.5 and 13.1 nm for WS_2 and MGr, respectively. Scale bar, 10 nm. (**E**) High-magnification TEM image of the ultrathin hBN tunnel barrier with a thickness of ~3 nm between the WS_2 and the graphene. (**F**) Measured histogram of the height distributions for hBN on SiO_2, confirming a height profile of <3 nm. Inset: AFM topographic image acquired from the device in (C) showing SiO_2 covered by hBN. a.u., arbitrary units. (**G**) XPS spectra of W 4f and B 1s core levels, located at 30 to 40 eV and 190 eV, respectively.

charge, the ideality factor, the Boltzmann constant, and the absolute temperature, respectively. In this way, a rectification ratio R_R of approximately 100,000 and η = 1.2 can be calculated. The R_R value obtained in our carristors represents at least a 10,000-fold improvement compared to other works investigating a p-n junction based on layer-by-layer stacked TMDs (*16*). We note that GW-B and GM-B performed within the limit in R_R, with a typical range of $<10^2$ (fig. S5), which is consistent with previous reports (*6*, *7*, *9*). The η value was found to be much smaller than that of TMD-based barristors (*6*), implying an optimal interface density of states (DOS) at the hBN-WS_2 interface. Such remarkable enhancements are expected to be a consequence of the substantial differences in the underlying principles of device physics.

The current rectifying behavior can be understood by examining the inset of Fig. 2A for $V_{TB} > 0$ (electron accumulation mode) and $V_{TB} < 0$ (hole inversion mode) biasing. The associated surface carrier density plot shown in Fig. 2B is consistent with this surface mode transition (see the Supplementary Materials for the calculation). Inversion- and accumulation-induced quasi-bound states, together with quantum confinement in the narrow quantum well near the WS_2 interface, were not characterized in this work but are probably the cause of the momentum-conserved transmission phenomenon. This part of the field is still relatively unexplored.

Although the electron wave function can penetrate a several-atom-thick hBN barrier resulting in a tunneling phenomenon due to barrier height $e\chi_{Tp}$ being much larger than the thermal energy, the conduction mechanism still needs to be elucidated and demonstrated using temperature-dependent transport measurements, as shown in Fig. 3A (the corresponding output data for GW-B are shown in fig. S6). The nearly flat out-of-plane resistivity of ~10^8 ohm·μm^2 [defined as $\rho^T = 1/(dJ_{TB}/dV)$, where J_{TB} is the current density] with decreasing temperature observed in Fig. 3B (MIS-C, blue squares) clearly indicates the tunneling behavior under the overall bias (*10*, *14*). Alternatively, GW-B (yellow squares) shows a significant decrease in ρ^T by more than four orders of magnitude from 230 to 90 K with semiconducting behavior and from 245 K to room temperature with strong metallic behavior. These two temperature regimes have also been observed by Georgiou *et al.* (*5*). Metal-semiconductor contact could be responsively adapted for the barristor and has indeed been extensively described by thermionic emission (*6*–*8*, *11*), thermionic field-emission (*8*), and FET models (*8*). Figure 3C presents an Arrhenius plot of $\ln(I_{TB})$ versus T^{-1} for the carristor (blue) and the barristor (yellow). It is interesting to note that that MIS-C has an ultralow activation energy E_A of 13 meV that is evidently smaller than k_BT (T = 300 K). E_A has a certain correlation with the temperature-dependent on/off ratio. The current component, owing to the disorder-assisted generation-recombination (G-R) effect in the depletion region (with width W_D) governed by Shockley-Read-Hall statistics, is expected to be temperature-sensitive (*14*) because it is proportional to $en_i(T)W_D/\tau$, where τ is the carrier lifetime and $n_i(T)$ is the intrinsic carrier density (see the Supplementary Materials). The measured E_A of the MIS-C is 100 times smaller than the half bandgap of WS_2; thus, the insignificant generation of G-R current is suggestive (*17*). We attribute the nonzero E_A to the

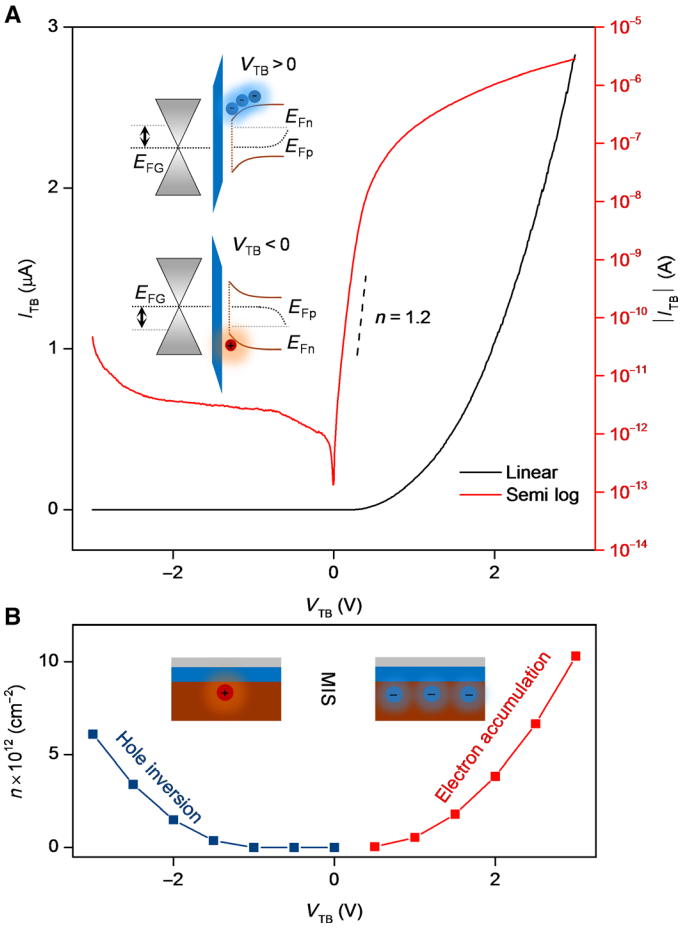

Fig. 2. Room temperature electrical characteristics of an MIS-C and energy band diagram. (**A**) I_{TB}-V_{TB} output curve measured across the heterostructure (between leads T1 and B) showing an ideality factor of 1.2; the silicon back gate was set to ground during the measurements. Inset: Schematic of the energy band diagram of a vertically stacked MIS-C under forward (top) and reverse (bottom) bias conditions. E_{FG}, graphene Fermi level; E_{Fn} (E_{Fp}), quasi-Fermi level for electrons (holes). (**B**) Calculated density of generated hole inversion and electron accumulation at the interface as a function of V_{TB} for an n-type WS_2. Note that the surface has weak inversion states at zero bias due to ϕ_{ms}.

bandgap reduction with temperature because of the intensified electron-phonon interaction at high temperatures that may alter the height of the barrier.

More surprisingly, the external electric field resulting from the silicon back gate determines the output characteristics. Figure 3D presents representative I_{TB}-V_{TB} curves for a V_G range of −7 to 7 V, allowing us to obtain R_R versus V_G over a range of 10 to 400,000 (inset of Fig. 3E). The nonlinear *I*-*V* curves are divided into two distinctive signatures, namely, current multiplication for $V_{TB} < 0$ and a plateau pattern for $V_{TB} > 0$. When $V_{TB} < 0$, we observed a marked current enhancement by more than five orders of magnitude. When $V_{TB} > 0$, as V_G is increased, a plateau can be clearly observed for each curve near zero V_{TB} that becomes more pronounced at large positive V_G. This plateau corresponds to the raising of the depletion layer in WS_2; that is, it provides evidence of (V_{TB},V_G)-dependent ϕ_s. We note that a flat form of ϕ_s weakens the generation of electron density at the WS_2 surface, leading to a nearly constant current region. Moreover, as ϕ_s departs from the flat band to shift down as V_{TB} increases, a large population of electrons allows all the curves to converge for a finite transmission coefficient T_E (*18*). We hypothesize that V_{TB}, V_G, variations in ϕ_s, and (constant) T_E play major roles in our MIS-C, as will be discussed in more detail. Generally, the amount of surface DOS acts as G-R centers and as an extra tunneling path between graphene and WS_2. Green *et al.* (*18*) have shown that the influence of surface DOS is substantial when the MIS-C is positively biased. However, the existence of a plateau confirms that the localized DOS has no detectable effect on the bandgap of the semiconductor, consistent with a recent study by Braga *et al.* (*19*). By contrast, GW-B and GM-B do exhibit current multiplication behavior (figs. S7A and S8A) that has been observed in other studies, but such behavior lacks the current-plateau feature.

Charge transport in MIS structures has been studied extensively because it is related to the planar MISFET (metal-insulator-semiconductor field-effect transistor) and is of primary importance to the reliability and stability of integrated circuit technology. By incorporating the Wentzel-Kramers-Brillouin approximation for rectangular barrier, the expression for the band-to-band current $I_{TB}(V_{TB}, V_G) \propto T_E exp[-e\phi_s(V_{TB}, V_G)/k_BT]$ was used to analyze the characteristics of the MIS-C (see the Supplementary Materials). We note that the MIS-C mimics the conventional MIS capacitor in that the band bending effectively depends on work function difference ϕ_{ms}, as mentioned above. Notably, we could electrostatically adjust the work function of graphene W_G to generate an undoubted transition in $\phi_s(V_{TB},V_G)$. It appears more directly, as displayed in Fig. 3E (left axis). Remarkably, by sweeping the polarity of V_G, $e\phi_s$ can be sensitively changed from 92 meV at $V_G = -7$ V to −205 meV at $V_G = 7$ V, suggesting the significant influence of $\phi_s(V_G)$ to form hole inversion and electron accumulation (see the Supplementary Materials for the ϕ_s extraction method). However, in the case of the GW-B, a positive value of $e\phi_B$ (from 459 to 313 meV) can be found over the entire range of V_G because the majority carrier transport is restricted only by ϕ_B (*7*–*9*, *11*). This finding for the GW-B complies with theoretical predictions (*20*, *21*) and experimental observation (*10*).

We define a barrier function $U_f = \ln(A^*AT^2T_E)$, where A^* and A are the Richardson constant and active contact area, respectively. Figure 3F shows that the measured value of U_f in our MIS-C is nearly independent of gate modulation at room temperature. Assuming the effective mass of a hole in hBN, $m^*_{BN} = 0.5m_0$ (*13*, *22*, *23*), and taking barrier thickness d_{BN} to be 2.8 nm, the theoretical model describes a calculated U_f (red circles in Fig. 3F) close to the measured value without the gating dependence, as expected, demonstrating an effective d_{BN} that is slightly smaller than ~3 nm (Fig. 1E). This observation reflects the lowering of the hole barrier behavior. Recent experimental efforts on tunnel devices with an hBN barrier embedded within different electrodes (graphene, graphite, and metal) have revealed discrepancies. The pronounced negative differential resistance with momentum transfer by aligning the crystal orientation of two graphene (*24*, *25*) or defect-assisted (*26*) Coulomb blockade signatures with defect-mediated tunneling (*27*) and that of the sublinear *I*-*V* curve with direct tunneling (*22*) is relatively ambiguous, although some of these devices contain identical graphene electrodes. Nevertheless, we did not observe resonant tunneling or single-electron charging effects in our samples; T_E exhibited the expected behavior of exponential dependence on d_{BN} and negligible barrier deformation as a function of V_G (see the Supplementary Materials).

We now explore the "transistor-like" operation of the MIS-C for the first time. Figure 4A illustrates the transfer characteristics (I_{TB}-V_G)

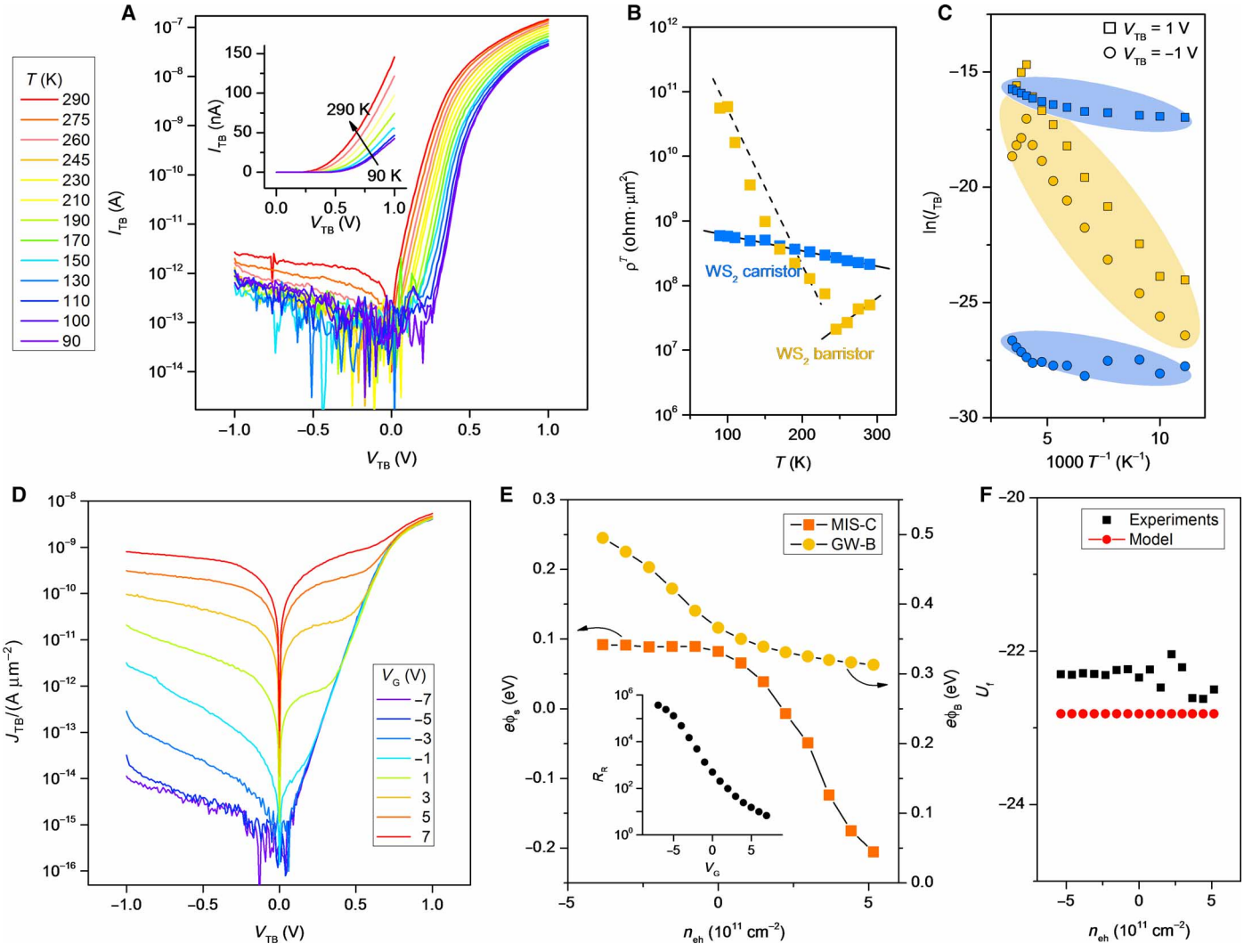

Fig. 3. Temperature- and electrostatic gating–dependent *I-V* characteristics. (**A**) Semilog I_{TB}-V_{TB} output curves of an MIS-C for temperatures between 90 and 290 K. Inset: The corresponding linear scale data. (**B**) Out-of-plane resistivity versus temperature curve for an MIS-C (blue) and a GW-B (yellow) at V_{TB} = 1 V. (**C**) Arrhenius plot of I_{TB} at V_{TB} = −1 V (circle) and 1 V (square) for an MIS-C (blue) and a GW-B (yellow). E_A of 108 meV for semiconducting and −155 meV for metallic behavior are extracted to yellow circles that are correlated to ϕ_B. (**D**) Semilog scale of I_{TB}-V_{TB} output curves for different back-gate voltages with an active contact area of 50 μm². (**E**) Surface potential (left axis) and Schottky barrier height (right axis) as functions of V_G modulation for MIS-C and GW-B, respectively. Note that ϕ_s has a saturation regime at V_G < 0 and becomes negative at V_G > 0. Inset: Rectification ratio as a function of V_G extracted from the data (D) at V_{TB} = ±1 V. (**F**) Barrier function as a function of 1000 T^{-1} in the temperature range from 90 to 290 K.

for a typical sample measured at V_{TB} = −0.5 V. A linear scale I_{TB}-V_G plot with various V_{TB} is displayed in the inset of Fig. 4A. We find that I_{TB} has an exponential dependence on V_G and a high on/off ratio of 3.6 × 10⁶ at V_{TB} = −0.5 V even at room temperature (see fig. S10 for different V_{TB} voltages), which is 100 to 100,000 times higher than the values reported in previous reports of graphene/TMD-based barristors (see figs. S7B and S8B for the results of our barristors) (*5*–*7*, *9*–*11*, *13*). Figure 4B depicts the corresponding asymmetric variation in ΔE_{FG} as a function of V_G. The asymmetry is probably caused by the unbalanced hole doping because the carrier counteraction occurs between the hole carriers doped by the negative polarity of V_G and the small amount of electron carriers created by negative V_{TB} (note that charge neutrality requires an equal charge at both sides of the semimetal and the semiconductor) (*14*). In addition, the preceding discussions assumed the ability to control the sequential tunneling of the double carriers. To further address this point, we fabricated MGr-based conventional FETs on SiO_2/Si wafer. The inset of Fig. 4C (top right) shows an optical image of the MGr-FET. A linear output behavior [inset of Fig. 4C (bottom)] confirms metal-to-MGr contact before in-plane resistivity ρ analysis. The associated ρ as a function of V_G presented a peak at the Dirac point voltage corresponding to the vanishing of the DOS as E_{FG} approached the Dirac point (Fig. 4C). Although different MGr FETs display different peak positions due to oxide charges and unintentional doping, the E_{FG} of MGr crosses over to the Dirac point (*28*, *29*). This behavior is similar to that of single-layer graphene (*28*).

On the basis of the benefits for the tunneling transport of MIS-C, as shown in Fig. 3A, weak temperature-dependent transfer characteristics

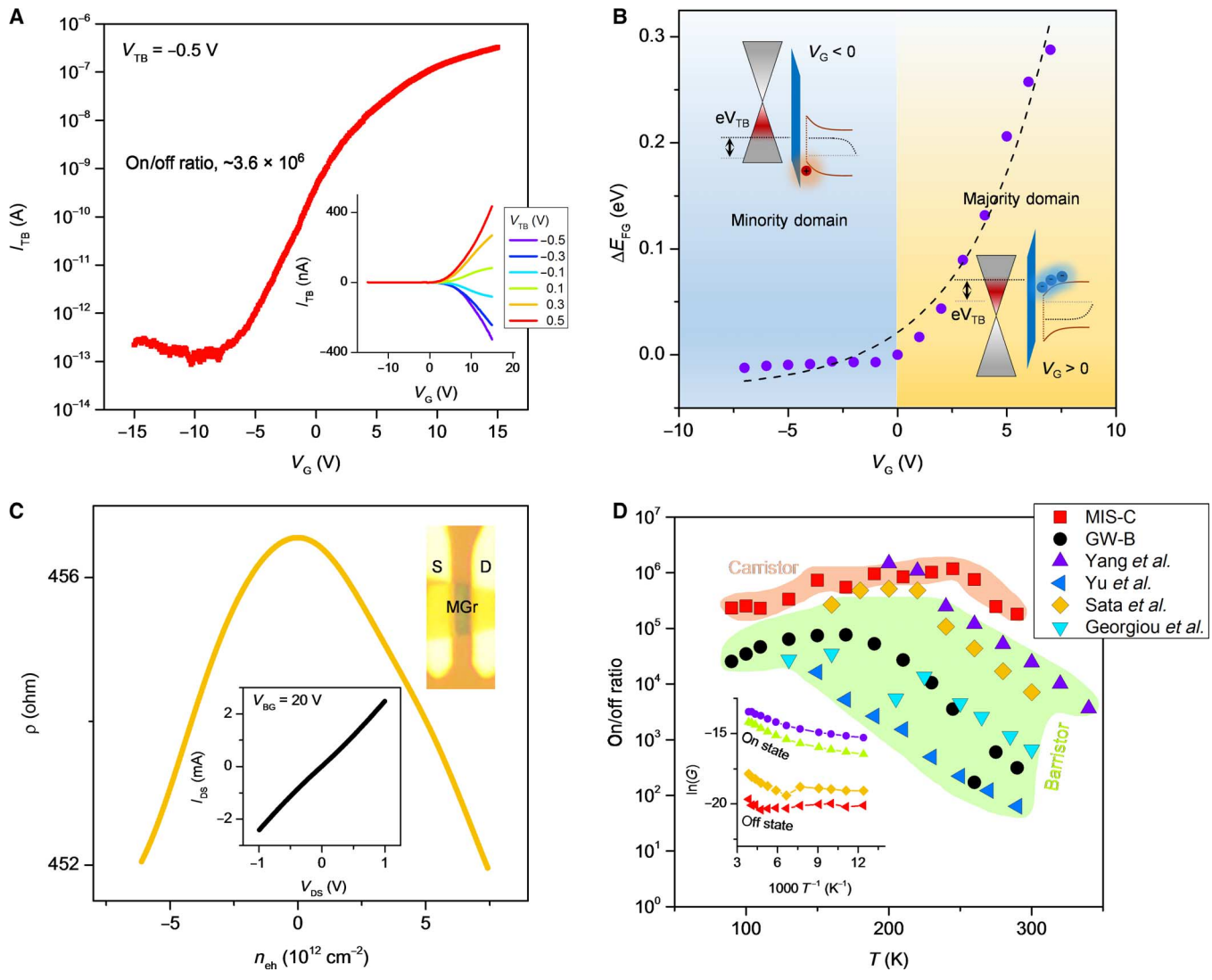

Fig. 4. Transfer characteristics of the carristor. (**A**) Room temperature semilog I_{TB}-V_G transfer characteristics of an MIS-C at V_{TB} = −0.5 V. Inset: The corresponding linear scale I_{TB}-V_G at various V_{TB}. (**B**) Fermi level shift of graphene versus V_G. These data are extracted from V_G-dependent surface potential variations and converted by applying the Schottky-Mott model based on the following expression: $\phi_s = W_G + \Delta E_{FG} - W_s$ (where W_s is the WS_2 work function). Inset: Energy band diagram under different gate polarities. Effect of p-doping (top; $V_G < 0$); the shifting of E_{FG} to a lower level results in ϕ_s forming an inversion layer; thus, I_{TB} is dominated by holes. Effect of n-doping (bottom; $V_G > 0$); the shifting of E_{FG} to an upper level results in ϕ_s forming an accumulation of electrons; I_{TB} is dominated by the abundance of electrons. (**C**) In-plane resistivity as a function of the gate voltage in an MGr channel FET measured at V_{SD} = 10 mV under room temperature. Insets: Output curve of the same device at a back-gate voltage V_{BG} = 20 V (bottom) and an optical image of a 10-nm-thick MGr with source/drain (S/D) contact (top right). (**D**) On/off ratio versus temperature for carristors and barristors. Inset: Plot of ln(*G*) versus 1000 T^{-1} for an MIS-C at on and off states, where conductance *G* is defined as $1/\rho^T$. The barristor data are extracted from previous studies (*5*, *6*, *9*, *11*).

should also be available. The electrostatic gating from the Si substrate is effectively screened by MGr (*29*, *30*) and only generates n- or p-doping in MGr. I_{off} and the on-state current I_{on} are similar to the current corresponding to negative and positive V_{TB}, respectively. The inset of Fig. 4D shows a plot of ln(*G*) versus 1000 T^{-1} in both on and off states, indicating that the observed behavior is in agreement with that of Fig. 3A. By using $\ln(I_{on}/I_{off}) \propto -E_A/k_BT$, the measured E_A in Fig. 4D (red squares) corresponds to approximately 11 meV, which is very close to the data extracted from Fig. 3C. In contrast, the GW-B exhibits an exponential decay with *T* (black circles) and a similarity in the decay slope to the results of other barristors (*5*, *6*, *9*, *11*). Their I_{off} response to temperature is analogous to the subthreshold conduction of silicon MISFETs (*12*). The expression $\ln(I_{on}/I_{off}) \propto -e\phi_B/k_BT$ is valid for describing Fig. 4D for barristors (*31*). We could roughly extract $e\phi_B$ of the barristors; typical values lay in the range of 148 to 303 meV.

DISCUSSION

To summarize, assembly of 2D crystals with atomic precision enables the creation of a novel carristor via layer-by-layer construction with materials having a distinctive electronic structure. Our assembly, the so-called carristor, exhibits current rectification and switching features and could open new routes for constructing electronic devices by taking advantage of the small active area (lack of double contact space

for S/D) and ultrafast direct tunneling time, which could enable the direct rectification of infrared radiation.

MATERIALS AND METHODS

Device fabrication

For the vertically stacked MGr-hBN-WS_2 (MIS-C) and MGr-TMD (GW-B and GM-B) devices, we used the standard Scotch tape–based cleavage technique for each 2D bulk crystal in combination with a contamination-free transfer method to avoid wet chemicals and even deionized water (*32*, *33*). Single-crystalline graphite was purchased from Graphene Supermarket, and hBN, WS_2, and MoS_2 were purchased from 2D Semiconductors. First, the bottom contact was prepatterned onto a degenerately doped Si substrate, followed by a 280-nm-thick SiO_2 capping layer, as shown in fig. S2A. Then, we applied mechanical exfoliation to obtain an MGr nanosheet that was deposited on a polydimethylsiloxane (PDMS) layer. Thick pieces of graphene with a typical thickness of 10 to 27 nm were chosen to create the bottom contacts, fully suppressing any underlying electric field screening (screening length of 1.2 nm) (*29*, *30*). This intermediate PDMS layer acted as a supporting framework for the transfer of 2D nanosheets by means of a micromanipulation system (*33*). After the MGr was placed at the desired location on the silicon substrate, we transferred an hBN nanosheet so that it overlapped the underlying MGr flake (fig. S2B). Subsequently, the top layer (WS_2 nanosheet) was placed onto the high-quality hBN that was used as both a tunnel barrier and an ultrasmooth, defect-free substrate (fig. S2C) (*34*). A 1.4-μm-thick layer of negative-tone photoresist was spin-coated onto the sample and patterned using a photomask through a photolithography process (fig. S2D). We metallized three separate top Ti/Au (10/60 nm) contacts for the vertical device using a thermal evaporator with a deposition rate of 5 Å/s. GW-B and GM-B have the same fabrication procedures but without inserting an hBN tunnel barrier for the direct MGr-TMD contact (fig. S3, A to D). Dozens of devices were fabricated and studied in the process of completing this study.

Materials characterization

High-resolution TEM images were obtained with a JEOL JEM-2100F operating at 200 kV. Before the TEM analysis, a focused ion beam (Quanta 3D FEG, FEI) was used to prepare site-specific samples (inset of Fig. 1D). The focused ion beam cutting and lift out were performed after the deposition of a carbon/Pt coating. The cross-sectional specimen was extracted from the studied device and used to determine the individual thicknesses of the layered materials and to verify the atomic sharpness of the interfaces. Topographic image and histogram statistics were carried out using an AFM (XE-100, Park Systems) in the noncontact mode of operation with an AR5-NCH (Nanosensors) cantilever. XPS core-level and valence band spectra were collected using an XPS (angle-resolved XPS, Thermo Fisher Scientific), incorporating a monochromatic Al Kα source (1486.6 eV). Energies of the spectra were calibrated against the C 1s peak set at 284.5 eV.

Electrical measurement

I-V characteristics were conducted using a semiconductor parameter analyzer (HP 4156A) and measured in a liquid nitrogen–cooled cryostat (ASK, 700 K) at a pressure of approximately 10^{-3} torr in a dark environment.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/4/e1602726/DC1

Supplementary Text

fig. S1. The 3D schematic structure of the carristor.

fig. S2. Optical images of MIS-C fabrication steps.

fig. S3. Optical images of GW-B (or GM-B) fabrication steps.

fig. S4. Band alignment of MIS-C and XPS spectra.

fig. S5. Schematic representation and *I-V* curves.

fig. S6. I_{TB}-V_{TB} curve for GW-B at different temperatures from 90 to 290 K V_G = 0.

fig. S7. Electrical transport characteristics of GW-B.

fig. S8. Electrical transport characteristics of GM-B.

fig. S9. Highly nonlinear dependence of I_{TB} as a function of V_{TB} for experimental (black line) and calculated data (red dots) under zero gate field and T = 300 K.

fig. S10. Semilog I_{TB}-V_G curves for MIS-C at different V_{TB} from −0.1 to −0.5 V at room temperature.

table S1. List of symbols and descriptions used in the study.

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