APPLIED SCIENCES AND ENGINEERING

A two-dimensional semiconductor transistor with boosted gate control and sensing ability

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Transistors with exfoliated two-dimensional (2D) materials on a SiO_2/Si substrate have been applied and have been proven effective in a wide range of applications, such as circuits, memory, photodetectors, gas sensors, optical modulators, valleytronics, and spintronics. However, these devices usually suffer from limited gate control because of the thick SiO_2 gate dielectric and the lack of reliable transfer method. We introduce a new back-gate transistor scheme fabricated on a novel Al_2O_3/ITO (indium tin oxide)/SiO_2/Si "stack" substrate, which was engineered with distinguishable optical identification of exfoliated 2D materials. High-quality exfoliated 2D materials could be easily obtained and recognized on this stack. Two typical 2D materials, MoS_2 and ReS_2, were implemented to demonstrate the enhancement of gate controllability. Both transistors show excellent electrical characteristics, including steep subthreshold swing (62 mV dec^{-1} for MoS_2 and 83 mV dec^{-1} for ReS_2), high mobility (61.79 $cm^2\ V^{-1}\ s^{-1}$ for MoS_2 and 7.32 $cm^2\ V^{-1}\ s^{-1}$ for ReS_2), large on/off ratio (~10^7), and reasonable working gate bias (below 3 V). Moreover, MoS_2 and ReS_2 photodetectors fabricated on the basis of the scheme have impressively leading photoresponsivities of 4000 and 760 A W^{-1} in the depletion area, respectively, and both have exceeded 10^6 A W^{-1} in the accumulation area, which is the best ever obtained. This opens up a suite of applications of this novel platform in 2D materials research with increasing needs of enhanced gate control.

INTRODUCTION

Two-dimensional (2D) layered materials, such as graphene and transition metal dichalcogenides (TMDCs), have emerged in recent years as an attractive class of materials for future electronic devices. Since the first report on a back-gate graphene transistor in 2004 (*1*), massive efforts to seek for high-quality materials and device fabrication of graphene and post-graphene TMDCs have been made. Monolayer and multilayer 2D materials can be obtained through different approaches, such as lithium-based intercalation (*2*), the hydrothermal method, and the "Scotch tape" method. Mechanical exfoliation has been widely used so far because of the simple and low-cost preparation of high-quality single-crystal 2D semiconductor samples with the least defects. Back-gate field-effect transistors (FETs) fabricated on the basis of the "Scotch-taped" samples have been extensively applied in devices such as logic circuits (*3*–*5*), memory (*6*), heterojunction transistors (*7*, *8*), photodetectors (*9*), gas sensors (*10*), and modulators (*11*). As a typical example of TMDC, MoS_2 has attracted lots of attention because of its unique electronic properties. Unlike zero-bandgap graphene (*1*, *12*), MoS_2 has a bandgap ranging from 1.29 to 1.8 eV, depending on its thickness (*13*, *14*). In particular, monolayer MoS_2 exhibits a direct bandgap of 1.8 to 1.9 eV (*15*), which makes it promising for optoelectronics applications. MoS_2 FETs have been proven to have excellent electrical performance under different ambient atmospheres and at varying temperatures (*16*–*18*). ReS_2 is a newly studied promising 2D material. Unlike other typical TMDCs with a thickness-dependent bandgap, ReS_2 has a direct bandgap regardless of material thickness from monolayer to bulk (*19*). Efficient light absorbing and emitting can thus be expected with monolayer and multilayer ReS_2. Recently published works have demonstrated that the photoresponse of the single-layer MoS_2 FET was found in the range of 400 to 680 nm and that the responsivity was calculated to be up to 880 A W^{-1} (*9*). The photoresponsivity of a ReS_2-based photodetector reached 88,500 A W^{-1} in the accumulation area (*20*).

In most works, exfoliated TMDC samples were taped onto a silicon substrate covered with a thick SiO_2 film (*5*, *9*, *20*–*26*) or a thick high-*k* dielectric (*27*) to build back-gate devices. The typical thickness of a SiO_2 layer is between 250 and 300 nm, so that it is easier to locate and roughly identify the layer number of the ultrathin TMDC flakes under an optical microscope (*1*). However, these FETs usually have poor gate control because of the thick gate dielectrics, and a high gate voltage (usually ≥40 V) is required to induce a substantial source-drain current (~1 μA) (*25*, *28*–*33*). One possible solution is to transfer the exfoliated sample from a SiO_2/Si surface to other desired substrates. Nevertheless, this high-quality transfer process still needs further improvement (*34*), because transfer processes usually involve spreading organic materials on the sample and following wet chemical etching, in which the ultrathin 2D semiconductor samples can easily be damaged, and contaminants can be introduced at the interface, leading to a degraded device behavior (*27*, *35*).

Here, we introduce a new device structure dedicated to breaking the limit of gate control and preserving the nondefect property at the same time. The structure consists of TMDC flakes exfoliated onto an Al_2O_3/ITO (indium tin oxide)/SiO_2/Si substrate. The thickness of an Al_2O_3/ITO/SiO_2 stack has been engineered to be 25 nm/70 nm/200 nm to ensure that the optical identification of exfoliated TMDC is very close to that of 300-nm SiO_2/Si. With the 25-nm Al_2O_3 layer as gate dielectric and ITO as back gate, FETs and photodetectors exhibited excellent electrical characteristics. Record low subthreshold swing (SS) and record high photoresponsivity have been obtained.

RESULTS

2D material–based back-gate transistors

Optical images of five MoS_2 flakes exfoliated on an Al_2O_3/ITO/SiO_2/Si substrate are shown in Fig. 1 (A to E). All the samples have a smooth surface without cracks or spots, and the flake size is larger

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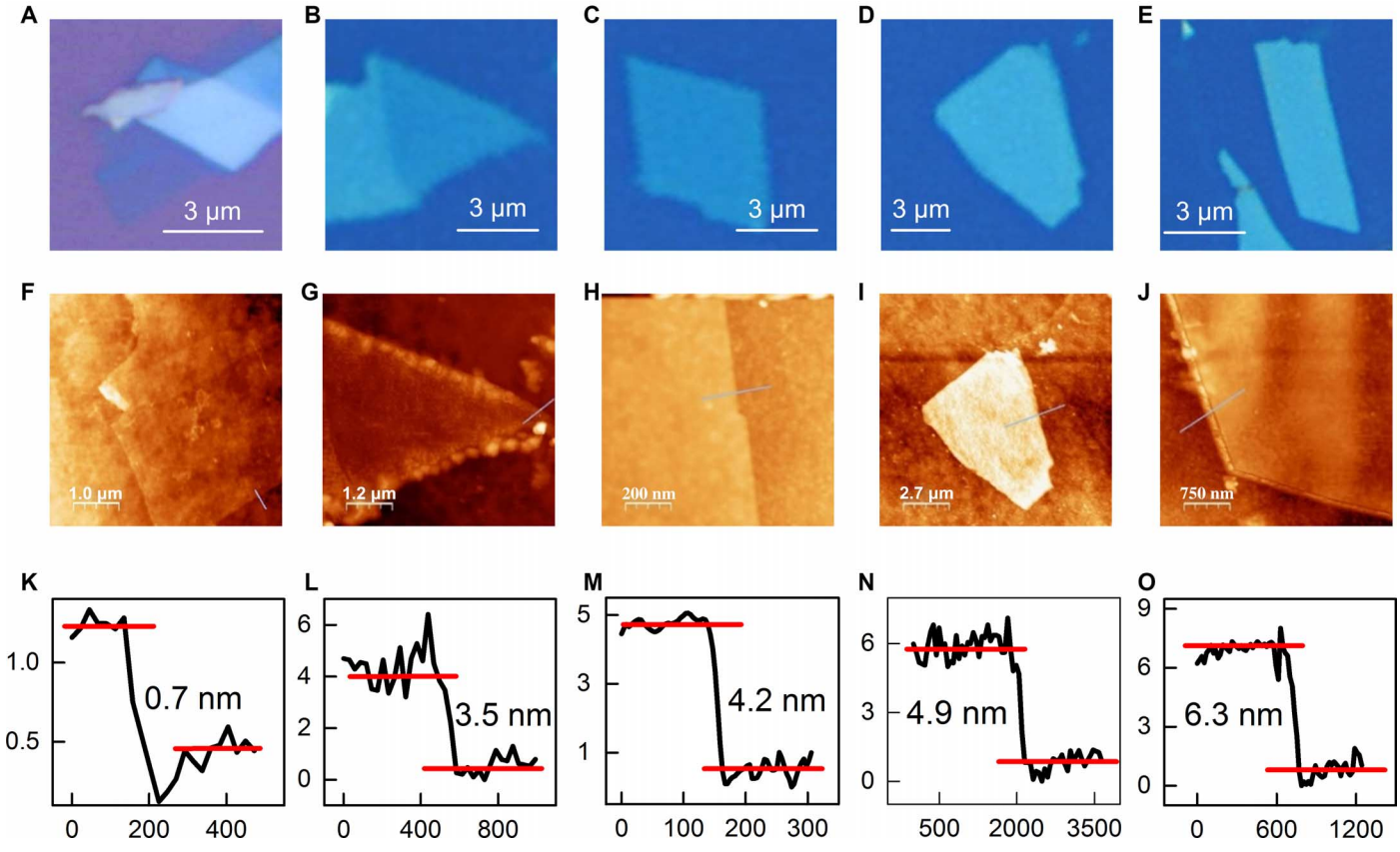

Fig. 1. Optical and AFM imaging of exfoliated MoS_2 materials on the Al_2O_3/ITO/SiO_2/Si substrate. (**A** to **E**) Optical images of five exfoliated MoS_2 flakes, with increasing thickness on the Al_2O_3/ITO/SiO_2/Si substrate. (**F** to **J**) AFM imaging of the five samples shown in (A) to (E). (**K** to **O**) Cross-sectional height profile obtained along the blue lines in AFM imaging shown in (F) to (J). The thicknesses of five MoS_2 materials in (A) to (E) were 2.1, 3.5, 4.2, 4.9, and 6.3 nm, respectively, indicating that these materials consist of three, five, six, seven, and nine layers, respectively.

than 10 μm^2, which is perfect for transistor fabrication. Atomic force microscopy (AFM) images and cross-sectional height profiles shown in Fig. 1 (F to O) indicate that all five samples are multilayer MoS_2 flakes, with thicknesses of 2.1 nm (three layers), 3.5 nm (five layers), 4.2 nm (six layers), 4.9 nm (seven layers), and 6.3 nm (nine layers). The abovementioned results suggest that the exfoliation and identification of MoS_2 flakes on the Al_2O_3/ITO/SiO_2/Si substrate are similar to those on the 300-nm SiO_2/Si substrate. The adoption of the exfoliation and identification of ReS_2 flakes on the Al_2O_3/ITO/SiO_2/Si substrate is also successful (fig. S1).

We built two back-gate transistors with a six-layer (6L) MoS_2 flake and a 4L ReS_2 flake. Figure 2A illustrates the schematic of the back-gate transistor and the measurement setup. The back-gate bias was directly applied on the ITO layer by probing through the Al_2O_3 gate dielectric. The TMDC channel was directly exposed to a light beam. Figure 2 (B and C) shows optical images of the 6L MoS_2 and 4L ReS_2 flakes on the Al_2O_3/ITO/SiO_2/Si substrate and the fabricated FETs. Electronic characterizations were performed at room temperature in air.

Figure 2 (D and E) shows the drain current (I_d) versus back-gate voltage (V_{bg}) transfer characteristics of MoS_2 and ReS_2 FETs. Unipolar, n-type field-effect behaviors have been observed in both transistors. Both devices have excellent transfer characteristics: small cutoff current (<1 pA), sharp turn-on, small gate leakage current (fig. S2), and large on/off current ratio (~10^7). The field-effect mobility extracted from I_d-V_{bg} curves was 61.79 $cm^2\ V^{-1}\ s^{-1}$ for MoS_2 and 7.32 $cm^2\ V^{-1}\ s^{-1}$ for ReS_2, and the SS of the MoS_2 and ReS_2 FETs was calculated to be as low as 62 and 83 mV dec^{-1}, respectively. It should be noted that there has been no report on exfoliated MoS_2 or ReS_2 back-gate FET with such small SS (typically >80 mV dec^{-1} for samples transferred on the desired substrate and ~1 V dec^{-1} for samples exfoliated on 300-nm SiO_2/Si) (*16*, *27*, *36*). Linear dependence of I_d on V_d at a low voltage level indicated ohmic Cr contact to MoS_2 and ReS_2 at source and drain (S/D) (Fig. 2, D and E, inset). A summary of the electrical performance of the transistors is shown in tables S1 and S2. This high performance with good mobility and excellent SS is due to the clean fabrication process and the enhanced gate control within a small range of gate voltage enabled by the Al_2O_3/ITO back-gate stack. This electrical performance is still impressive even when compared with most reported work on the top-gate TMDC transistors (tables S3 and S4). The TMDC/Al_2O_3/ITO/SiO_2/Si structure provides an alternative and promising device platform toward the back-gate TMDC device application with enhanced gate control. (Top-gate MoS_2 FET was further fabricated on the basis of the device platform, and a detailed comparison is shown in fig. S3.)

2D material–based photodetectors

To study the effect of enhanced gate control on the 2D material's sensing ability, another back-gate FET was fabricated on the basis of single-layer MoS_2 with direct bandgap on the Al_2O_3/ITO/SiO_2/Si substrate, to perform optical-electrical characterization. The Raman and photoluminescence spectra of single-layer MoS_2 are shown in

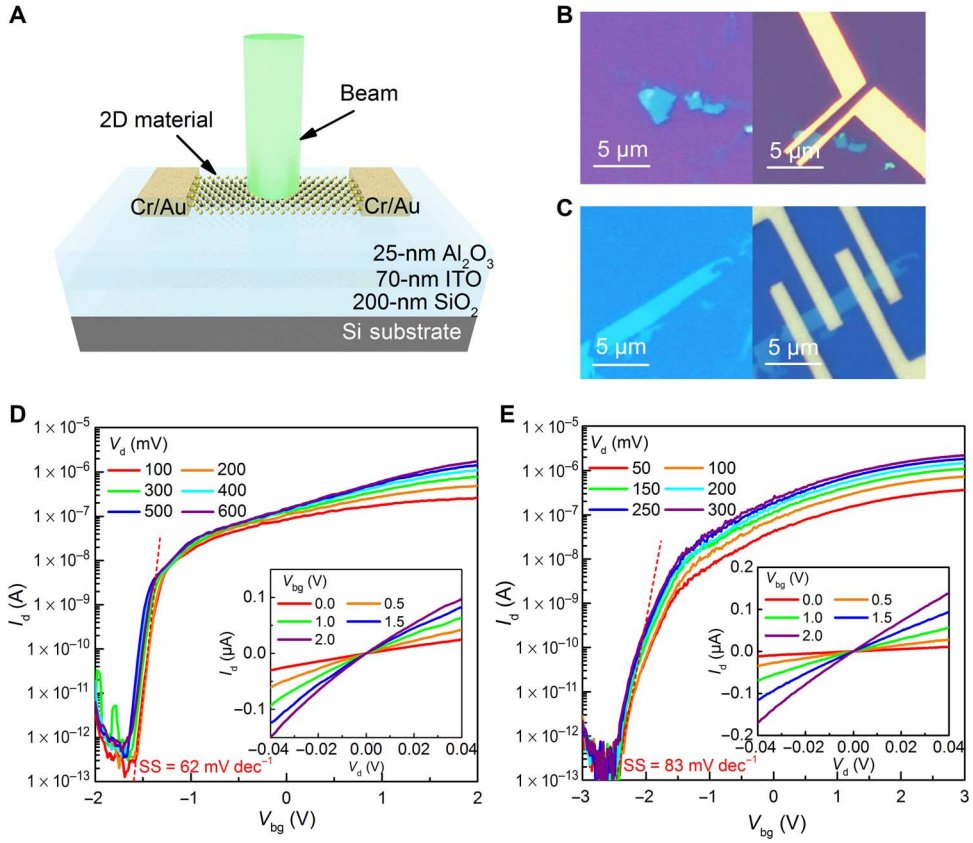

Fig. 2. Structure and electrical characterization of exfoliated MoS_2 and ReS_2 transistors. (**A**) Schematic of a FET on Al_2O_3/ITO/SiO_2/Si and the measurement setup. (**B**) Optical image of MoS_2 and the fabricated transistor. (**C**) Optical image of ReS_2 and the fabricated transistor. (**D**) MoS_2 FET: I_d-V_{bg} transfer curves in log scale, with V_d ranging from 100 to 600 mV. The transistor showed a small cutoff current (<1 pA) and a large on/off ratio (~10^7). The calculated electron mobility and SS were 61.79 $cm^2\ V^{-1}\ s^{-1}$ and 62 mV dec^{-1}, respectively. Inset: I_d-V_d curves swept from −40 to 40 mV under different V_{bg}. The symmetric curves indicate ohmic contact at S/D. (**E**) ReS_2 FET: I_d-V_{bg} transfer curves in log scale, with V_d ranging from 50 to 300 mV. The calculated electron mobility and SS were 7.32 $cm^2\ V^{-1}\ s^{-1}$ and 83 mV dec^{-1}, respectively. Inset: I_d-V_d curves swept from −40 to 40 mV under different V_{bg}. The symmetric curves indicate ohmic contact at S/D.

Fig. 3 (A and B), and the optical and AFM images are shown in fig. S4. The electron mobility and SS of the single-layer MoS_2 transistor extracted from Fig. 3C were calculated to be 6.84 $cm^2\ V^{-1}\ s^{-1}$ and 96 mV dec^{-1}, respectively. The device was measured as an n-type photodetector, and Fig. 3C shows the drain current excited by the light beam under different power. The results indicated that a distinct photocurrent can be observed even with a light intensity increase in the femtowatt level. The single-layer MoS_2 FET showed high sensitivity in visible wavelength (Fig. 3D). By taking the current values obtained at V_{bg} = 0.5, 0.8, and 1.2 V for depletion, subthreshold, and accumulation areas, respectively, the photoresponsivity was calculated up to 4000 A W^{-1} in the depletion area and 123,000 A W^{-1} in the accumulation area, with V_d = 1 V (comparison with a previous report is shown in table S5). The on/off ratio of the photocurrent was around 670 in the depletion area, 32 in the subthreshold area, and 2.2 in the accumulation area. The time-resolved photocurrent response of a single-layer MoS_2 photodetector is shown in fig. S5. These results are similar to those obtained from a previously reported n-channel MoS_2 photodetector (*9*, *26*).

Similar optical-electrical characterization was also performed with the 4L ReS_2 FET. The Raman and photoluminescence spectra of 4L ReS_2 are shown in Fig. 4 (A and B), and the optical and AFM images are shown in fig. S4. Results in Fig. 4C indicated that the ReS_2 FET was less sensitive than the single-layer MoS_2 FET in the depletion area. The ReS_2 FET on the Al_2O_3/ITO/SiO_2/Si substrate also has a broad sensitivity in visible wavelength, as shown in Fig. 4D. The photoresponsivity of the ReS_2 FET in Fig. 4 (D and E) was only $^1/_{10}$ of the single-layer MoS_2 FET in the depletion area, which also confirmed the previous conclusion. The photoresponsivity of the ReS_2 FET was calculated up to 760 A W^{-1} in the depletion area and 503,000 A W^{-1} in the accumulation area, with V_d = 1 V. The on/off ratio of the photocurrent was around 50 in the depletion area, 8 in the subthreshold area, and 1.2 in the accumulation area. The time-resolved photocurrent response of a 4L ReS_2 photodetector is shown in fig. S6. These results are similar to those obtained from a previously reported n-channel ReS_2 photodetector (*20*, *37*).

DISCUSSION

Here, the Al_2O_3/ITO/SiO_2 stack has been engineered such that exfoliated 2D material flakes with different thicknesses can be obtained similar to those obtained from the 300-nm SiO_2/Si substrate for device fabrication. Excellent device characteristics have been obtained using TMDCs as channel and ITO as back gate, including large on/off ratio (~10^7), high electron mobility (61.79 $cm^2\ V^{-1}\ s^{-1}$ for MoS_2 and 7.32 $cm^2\ V^{-1}\ s^{-1}$ for ReS_2), and small SS (62 mV dec^{-1} for MoS_2 and 83 mV dec^{-1} for ReS_2). These excellent properties have outperformed

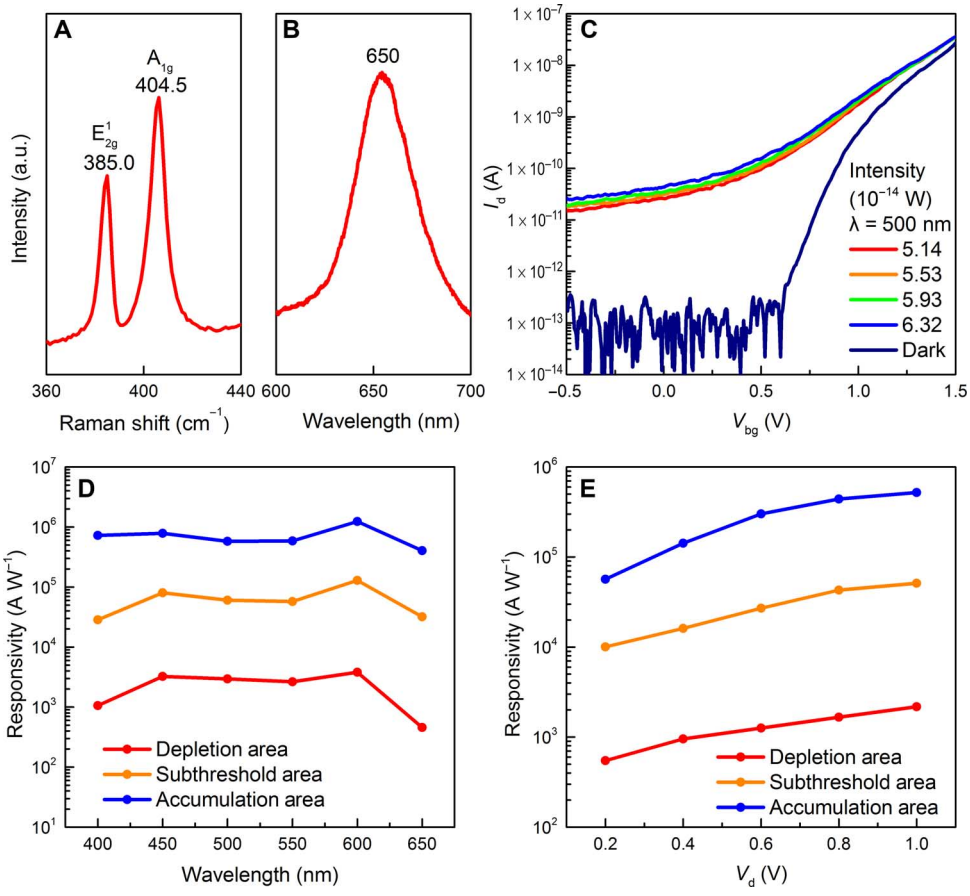

Fig. 3. Optical-electrical characterization of a single-layer MoS_2 photodetector on the Al_2O_3/ITO/SiO_2/Si substrate. Raman (**A**) and photoluminescence (**B**) spectra of single-layer MoS_2. a.u., arbitrary units. (**C**) I_d-V_{bg} transfer curves in log scale, with different light power and dark current. (**D**) Photoresponsivity versus wavelength in log scale in depletion, subthreshold, and accumulation areas. (**E**) Photoresponsivity versus V_d in log scale in depletion, subthreshold, and accumulation areas.

most reported back-gate MoS_2 and ReS_2 FET performances and are comparable to those of reported top-gate FETs (tables S3 and S4). The lowest reported SS for a 2D material back-gate transistor was 70 mV dec^{-1} (*27*); however, the exfoliated MoS_2 in this study was more than 10 nm thick, which could hardly be called a "2D" material.

The back-gate transistor structure is crucial to 2D material intrinsic property research, including discovering excellent 2D semiconductor candidates (*1*, *38*) and studying band structure or valleytronics (*15*), as well as all kinds of semiconductor devices such as logic circuits (*3*–*5*), memory (*6*), heterojunction transistors (*7*, *8*), photodetectors (*9*), gas sensors (*10*), and modulators (*11*). The 2D material on the Al_2O_3/ITO/SiO_2 stack can be more sensible to weak electric signal or atmosphere change, on and off in a small range of gate bias, and less power-consuming because the gate control is greatly improved. This manuscript provided a reasonable example to show the superiority of this material in the enhancement of photoresponsivity. In addition, we chose two typical 2D materials, MoS_2 and ReS_2, to be fabricated into photodetectors to prove that this structure could be applied to all 2D semiconductor research.

The photodetectors in this study were fabricated with single-layer MoS_2 and 4L ReS_2, showing impressive photoresponsivities of 4000 and 760 A W^{-1} in the depletion area, respectively, and more than 10^6 A W^{-1} for both in the accumulation area, which is almost five times higher than the previously reported highest responsivity (*9*). The high responsivity benefits from enhanced gate controllability. In the depletion area, negative bias will cause band bending in the channel (fig. S7B). Compared to the photodetectors on the 300-nm SiO_2 dielectric, the band bending in the channel of the photodetectors on the Al_2O_3/ITO substrate is strengthened when the gate bias is the same, and as a result, the electric field, which is the derivative of band bending, is stronger in the channel directions of the devices on the Al_2O_3/ITO substrate. A stronger electric field could result in carriers excited by photons reaching S/D at a higher speed and greatly enhances the photocurrent. The light reflection between dielectrics also plays an important role in boosting sensibility. Traditional exfoliated n-channel MoS_2 photodetectors were fabricated on 300-nm SiO_2, and as a result, only a small portion of light could be reflected at the SiO_2/Si interface. Most of the light was absorbed by the silicon substrate, because silicon had a high index of refraction of 3.4 and could absorb light in visible wavelength. Nevertheless, the Al_2O_3/ITO/SiO_2 stack had an index of refraction of 1.63:2.10:1.46 on the surface, which could reflect most incoming light through the interfaces before light reached the silicon substrate. Thus, the 2D material on the Al_2O_3/ITO/SiO_2 stack could absorb far more light and generate more carriers than those on the SiO_2/Si substrate, leading to a significant increase in photoresponsivity (fig. S7, C and D). In summary, the device structure with novel Al_2O_3/ITO/SiO_2 stack engineering has provided a great platform with enhanced gate control and electrical performance for further investigations on other 2D material–based back-gate FET applications in a

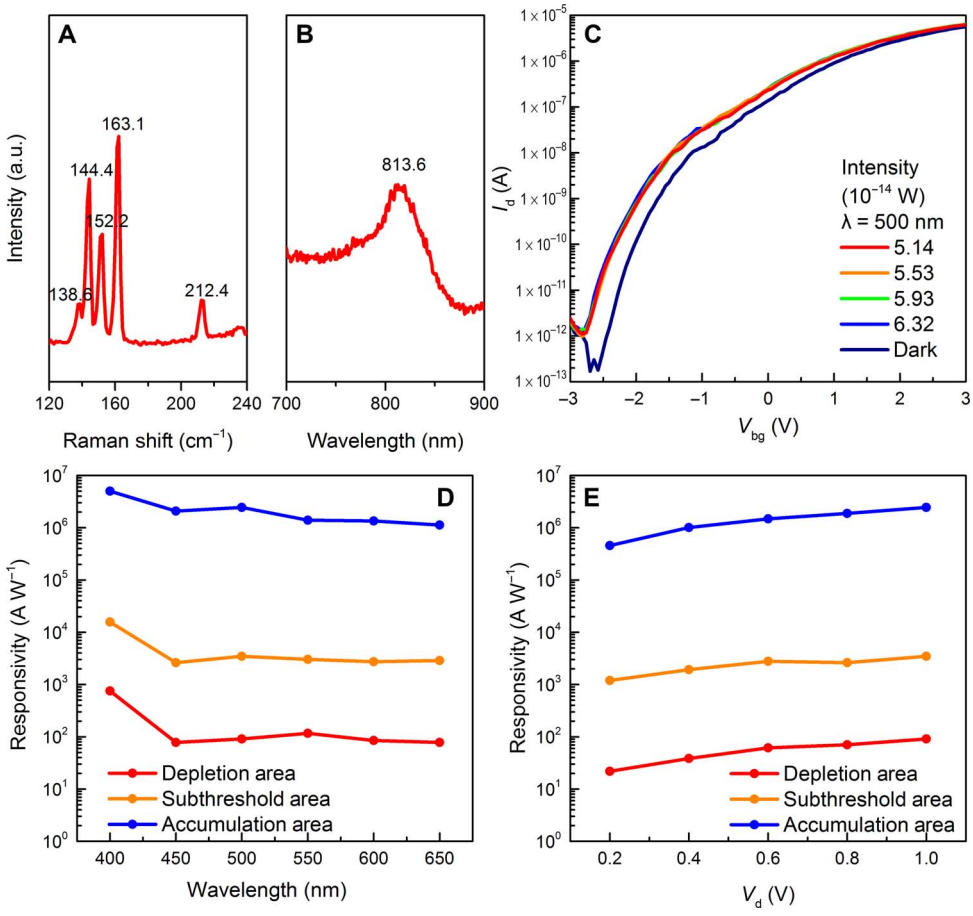

Fig. 4. Optical-electrical characterization of a 4L ReS_2 photodetector on the Al_2O_3/ITO/SiO_2/Si substrate. Raman (**A**) and photoluminescence (**B**) spectra of 4L ReS_2. (**C**) I_d-V_{bg} transfer curves in log scale, with different light power and dark current. (**D**) Photoresponsivity versus wavelength in log scale in depletion, subthreshold, and accumulation areas. (**E**) Photoresponsivity versus V_d in log scale in depletion, subthreshold, and accumulation areas.

number of fields, such as materials physics, logical circuits, optoelectronics, and sensing devices.

MATERIALS AND METHODS

Experimental design

A 200-nm SiO_2 layer was first grown on a heavily doped silicon substrate by dry oxidization. Then, a layer of a 70-nm ITO film was deposited directly on SiO_2 by sputtering, followed by annealing at 300°C for 15 min to lower the ITO film resistance. The radio frequency (rf) power of ITO sputtering was 120 W, and the deposition time was 550 s.

A 25-nm Al_2O_3 layer was subsequently deposited with atomic layer deposition (ALD) at 300°C. multilayer TMDC samples were then mechanically exfoliated by using the Scotch tape method onto the Al_2O_3/ITO/SiO_2/Si substrate. A bulk MoS_2 crystal was purchased from SPI Supplies, and a bulk ReS_2 crystal was purchased from HQ Graphene. We chose flakes without apparent spots or cracks and over 10 μm^2 in size as it would otherwise be difficult to deposit metal electrodes on the flakes.

The next step was to pattern the S/D electrodes with electron beam lithography and deposit 10 nm/70 nm Cr/Au to form S/D contacts. The width of the S/D electrodes was 1 μm for MoS_2 and 2 μm for ReS_2. Cr/Au contacts were deposited by sputtering, at an rf power of 80 W. Then, an O_2 plasma treatment was performed with an rf power of 30 W for 30 s to remove possible contaminants on the surface. A comparison of the electrical characterization and Raman spectrum of MoS_2 and ReS_2 FETs is shown in fig. S8. The length and width of the MoS_2 channel were 2.5 and 4 μm, respectively, whereas those of the ReS_2 channel were 1 and 2 μm, respectively.

The dual-gate MoS_2 transistor was prepared as follows: The back-gate MoS_2 transistor was first fabricated, followed by an immediate deposition of 30-nm Al_2O_3 with ALD. Then, the top-gate electrode was fabricated using the same technique as that used for S/D electrodes. The width of the top-gate electrode was 0.8 μm. The final device was annealed at 350°C in forming gas (5% H_2 in N_2) to remove possible photoresist residues and improve the metal contact to the MoS_2 flake. The optical image and electrical characterization of the dual-gate MoS_2 transistor are shown in fig. S3.

Electrical and optical measurement

AFM imaging was performed in air before back-gate transistor fabrication. The AFM images were processed by WS_xM 5.0 Develop 8.1. Raman spectroscopy and photoluminescence spectroscopy were performed in air after back-gate transistor fabrication, at a wavelength of 532 nm and with a light spot of 0.8 μm.

The electrical characterization of MoS_2 and ReS_2 FETs was carried out with an Agilent B1500A semiconductor analyzer at room temperature in air. Back-gate contact was performed by probing through the Al_2O_3

dielectric on the surface to reach the ITO layer. The optical-electrical measurement was performed using the same semiconductor analyzer and under the same test environment as those of the electrical characterization measurement. An additional light source was placed on the top of MoS_2 and ReS_2 FETs, and then, all apparatuses were put in a dark box to get rid of other incoming light. The light beam was generated from a high-power filament lamp, whose filament current could be adjusted to between 17 and 20 A. The light beam went through a monochromator and then through an optical fiber. The light intensity was measured by a light intensity meter and was converted to light power according to the size of the light spot and the size of MoS_2 and ReS_2 channels.

We carried out several electrical characterizations at the beginning of the test to ensure that the cable connection was stable. The data in this study were all measured as soon as the device was fabricated. Degeneration in performance was observed after the device was put in air for several weeks.

The whole experiment is reproducible. We have fabricated more than one MoS_2 or ReS_2 back-gate transistor on this new substrate.

Statistical analysis

All curves in this study were measured by an Agilent B1500A semiconductor analyzer. There were 101 points in each curve. The sampling rate was 1 Hz, which was low enough to be regarded as a dc test.

The data plotted in the figures are all raw data. No denoise, smooth, or similar methods were taken. The field-effect mobility extracted from the I_d-V_{bg} curve was based on the following equation

$$\mu = \frac{dI}{dV}\frac{\dot{L}}{C_{ox}W}\frac{\dot{1}}{V_{ds}} = \frac{dI}{dV}\frac{\dot{d_{ox}}L}{\varepsilon_0\varepsilon_r W}\frac{\dot{1}}{V_{ds}}$$

where ε_0 is vacuum permittivity. The gate dielectric in both MoS_2 and ReS_2 transistors was the 20-nm Al_2O_3 layer grown via ALD; thus, d_{ox} = 20 nm and ε_r = 6.4. The electron mobility was calculated by the maximum of $\frac{dI}{dV}\frac{\dot{1}}{V_{ds}}$ in the I_d-V_{bg} curves.

The switching performance of the transistor was characterized by the SS, which is defined as the V_{bg} swing to achieve a 10-fold increase of I_d in the subthreshold region, on the basis of the following equation

$$SS = \frac{dV}{d\log_{10}I}$$

We calculated the mean of SS in each decade of drain current.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/3/5/e1602246/DC1

Electrical characterization of back-gate ReS_2 and dual-gate MoS_2 transistors on the Al_2O_3/ITO/SiO_2/Si substrate

Optical-electrical characterization of MoS_2 and ReS_2 transistors

Low-power O_2 plasma treatment

Property of multilayer ReS_2

Photoresponsivity of MoS_2 and ReS_2 photodetectors

fig. S1. Optical and AFM images of multilayer ReS_2.

fig. S2. Gate leakage current of a transistor on the Al_2O_3/ITO/SiO_2/Si substrate.

fig. S3. Electrical characterization of top-gate MoS_2 transistor.

fig. S4. Optical and AFM images of single-layer MoS2 and 4L ReS2 photodetectors.

fig. S5. Time-resolved photocurrent response of a single-layer MoS_2 photodetector.

fig. S6. Time-resolved photocurrent response of a 4L ReS_2 photodetector.

fig. S7. Schematic of a 2D material photodetector on the Al_2O_3/ITO/SiO_2/Si substrate.

fig. S8. Electrical characterization and Raman spectrum comparison between before and after low-power O_2 plasma treatment.

fig. S9. I_d-V_d curves of MoS_2 and ReS_2 transistors with different V_{bg}.

fig. S10. Raman and photoluminescence spectra of multilayer ReS_2.

fig. S11. Optical-electrical characterization of a single-layer MoS_2 photodetector.

fig. S12. Optical-electrical characterization of a single-layer ReS_2 photodetector.

table S1. Electron mobility, SS, and on/off ratio of five different MoS_2 back-gate transistors.

table S2. Electron mobility, SS, and on/off ratio of five different ReS_2 back-gate transistors.

table S3. Summary of back-gate and top-gate exfoliated MoS_2 transistor electrical characterization in related reports.

table S4. Summary of back-gate and top-gate exfoliated ReS_2 transistor electrical characterization in related reports.

table S5. Summary of photoresponsivity of 2D material photodetectors in related reports.

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