

APPLIED SCIENCES AND ENGINEERING

Multichannel parallel processing of neural signals in memristor arrays

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Fully implantable neural interfaces with massive recording channels bring the gospel to patients with motor or speech function loss. As the number of recording channels rapidly increases, conventional complementary metal-oxide semiconductor (CMOS) chips for neural signal processing face severe challenges on parallelism scalability, computational cost, and power consumption. In this work, we propose a previously unexplored approach for parallel processing of multichannel neural signals in memristor arrays, taking advantage of their rich dynamic characteristics. The critical information of neural signal waveform is extracted and encoded in the memristor conductance modulation. A signal segmentation scheme is developed to adapt to device variations. To verify the fidelity of the processed results, seizure prediction is further demonstrated, with high accuracy above 95% and also more than 1000× improvement in power efficiency compared with CMOS counterparts. This work suggests that memristor arrays could be a promising multichannel signal processing module for future implantable neural interfaces.

INTRODUCTION

Electrical monitoring of brain activities has been proved to be an effective approach to probe the underlying neural principles and has broad applications in biomedical fields (1–7). Invasive neural probes, microelectrodes arrays, or electrode grids with vast recording channels are popular tools to record brain activities (8–13). In recent years, the amount of recorded neural signal data accumulates explosively with the exponentially increasing number of recording channels (14, 15), and it poses a critical challenge for real-time processing of multichannel neural signals (1, 4, 16–18). Most existing signal processing hardware systems rely on multiplexing multiple recording channels to single or several processing units to carry out heavy computation tasks (Fig. 1A) (2, 5, 13). However, these systems have inherent scalability issues because of the delay and power consumption incurred by multiplexing. These issues further limit many practical biomedical applications that usually require more recording channels, such as disease diagnosis and neural interfaces. In these scenarios, new devices and hardware systems are urgently demanded to process multichannel neural signals in parallel, especially those that can directly extract and store critical information from neural signals in a highly efficient manner.

Memristor, an emerging neuromorphic device, has shown great potential in energy-efficient data processing owing to its capability of exploiting inherent physical attributes to implement computations (19–25). In literature, memristor array-based vector-matrix multiplications based on the Ohm's law and Kirchhoff's law have been widely demonstrated (23, 26–28). Besides, the rich dynamics in memristor associated with physical state changes could be used to realize logic operations (29, 30) and also temporal correlation detections (31), where the computation results are often directly stored

in the devices. The latter approach is appealing for real-time neural signal processing with low power consumption. An early proposal for this application is the demonstration of detecting neuronal spikes using the inherent over-threshold integrating characteristics of TaO_x-based memristor (32). However, because of the inevitable device-to-device variations and the saturation behavior of device resistances (33), it is difficult to directly apply this method to multiple recording channels for parallel processing. Moreover, it may not be feasible to process another important kind of neural signals—local field potential (LFP) (34), which reflects the summation of postsynaptic potentials of neuronal population (34) and is essential in neuroscience and many medical applications like epilepsy diagnosis (17, 35–37). LFP might be more suitable than neuronal spikes for low-power biomedical electronics because of its relatively low sampling rate (35, 38). It also has richer signal dynamics than neuronal spikes; therefore, more complex computation, rather than amplitude threshold detection as in neuronal spikes, is required to extract its key information (5). Intracranial electroencephalography (iEEG) is a typical method to record LFPs by using electrodes on the brain surface or inside the brain, and iEEG signals are often collected from patients with epilepsy (37), which is one of the most common neurological disorders (39). Epilepsy seizure prediction helps develop new therapeutic strategies for epilepsy, and it requires the ability to differentiate the preictal and interictal states to give patients pre-seizure warnings or deliver preemptive therapy (40). For this purpose, multichannel parallel processing of LFPs based on the memristor dynamics could be an attractive approach to predict epilepsy seizures, which has not yet been experimentally demonstrated so far.

Here, we propose a system for parallel processing of multichannel LFPs using one transistor–one resistor (1T1R) memristor array (Fig. 1B and fig. S1). This system uses the inherent memristor conductance modulation to extract the energy and variation information of the input neural signals. Signal segmentation schemes in the memristor array are realized via the 1T1R architecture to retain more input information and also accommodate the device-to-device variations. To validate the feasibility of the proposed system, 16-channel iEEG signals are used as the neural signals to be processed. In addition,

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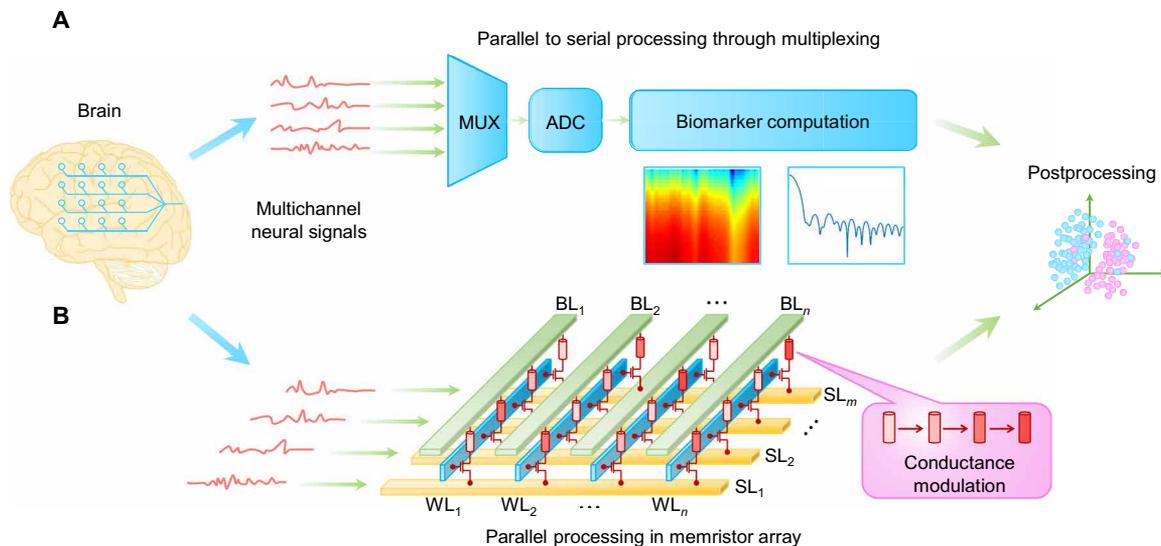


Fig. 1. Multichannel neural signal processing systems. (A) Illustration of conventional neural signal processing systems, which often use multiplexers (MUXs) to transform multichannel neural signals to serial signals and then process them for biomarker computation. (B) The proposed memristor-based system, which uses a memristor array for parallel processing of multichannel neural signals where the biomarker extraction is achieved by memristor conductance modulations. BL, bit line; WL, word line; SL, source line.

high-accuracy seizure prediction based on the processed results is demonstrated.

RESULTS

Distinguish signal waveforms by memristor conductance modulation

A 1k-cell cross-point array of memristors with TiN/TaO_x/HfO_y/TiN material stack is fabricated (see Materials and Methods for the fabrication details) as the platform to process multichannel neural signals in parallel. Here, the TaO_x layer serves as the thermal enhanced layer to improve the analog conductance modulation behaviors of HfO_y-based memristor, whose conductance states can be gradually modulated by applying electrical stimuli. Each cell has a 1T1R structure, as shown in fig. S2A, where the memristor stack sits on top of the transistor drain terminal [bit line (BL)]. The gate and source terminals are connected to the word (WL) and source lines (SL), respectively. Figure 2A shows the analog conductance modulation under 15 identical RESET voltage pulses through SL ($V_{SL} = 1.3$ to 1.8 V, $V_{WL} = 5.0$ V, and $V_{BL} = 0$ V) starting from the same initial conductance value. Similarly, fig. S2B shows the results for the SET processes. Different colored lines represent different pulse amplitudes. It can be seen that the memristor conductance modulation processes are highly correlated with the amplitudes of input pulses. When the pulse amplitudes increase, the conductance decreases faster and tends to saturate at lower values, so the memristor can distinguish different input signal energies.

Besides signal energies, the memristor could also distinguish different input signal waveforms, such as variations. To validate this statement, four groups of 15-pulse trains with the same average amplitude of 1.5 V (i.e., the same signal energy) but different SDs σ (i.e., different signal variations) are applied to modulate the memristor conductance (Fig. 2B). As we can see, different conductance evolution processes are observed for different input signal waveforms (Fig. 2C). Relatively larger conductance changes (ΔG) are usually

observed after the pulse with higher amplitude in each pulse train (indicated by arrows), so signals with larger variations would cause larger ΔG in the final conductance, as shown in Fig. 2D. This conductance modulation behavior is crucial for neural signal processing, as it helps to extract the critical information of both energies and variations of the input signal and encode them into the memristor conductance change. It is noteworthy that this important information is automatically stored in the nonvolatile memristor and can be accessed as device conductance states through read operations for feature extractions later. This is the foundation for the following parallel processing of neural signals.

Parallel multichannel neural signal processing

To parallel process multichannel neural signals, a signal segmentation scheme is developed on the basis of our memristor array, as shown in Fig. 3A. Raw signals collected from the brain are first linearly transformed (with amplification and offset) to the desired voltage ranges (i.e., ~ 1 to 2 V) and then used as the input signals for the memristor array following

$$V_{in} = V_{raw} \times \text{Gain} + V_{offset} \quad (1)$$

The transformed multichannel signals, each lasting for about 2.4 s, are fed into the multiple rows of the memristor array. The 64 columns are then turned on sequentially by the WLs, so that the input signals in each channel are divided into segments with identical length (37.5 ms) to apply on the corresponding column of memristors, whose conductance changes record the energy and variation information of the input signals. Here, the signal sampling rate is 400 Hz, so each segment corresponds to a 15-pulse train, similar to the test waveform in Fig. 2B. This signal segmentation scheme in the memristor array with 1T1R architecture allows it to store the information of input signal evolution with time. In practice, the size of the required memristor array can be determined by the number

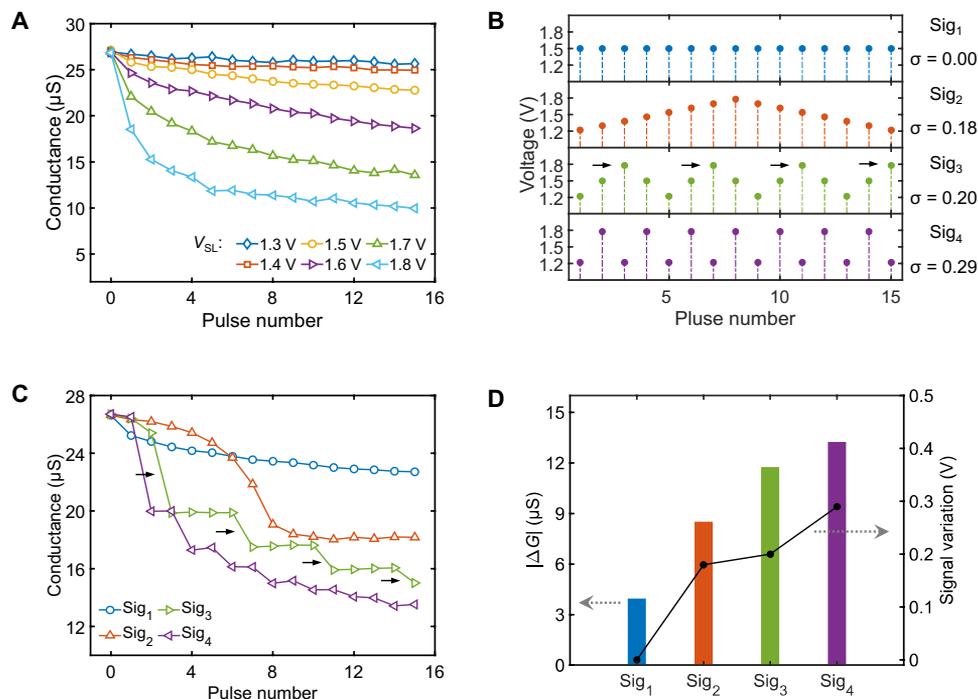


Fig. 2. Distinguish signal waveforms through memristor conductance modulation. (A) Memristor conductance modulation process under multiple identical RESET pulses starting from the same initial conductance value. Each data point is averaged from 128 devices. $V_{\text{WL}} = 5.0$ V and $V_{\text{BL}} = 0$ V. Pulse width, 50 ns. (B) Waveforms of several designed input signal pulse trains. They have the same average amplitude of 1.5 V, but different variations (σ), which increase from top to bottom. σ unit: volts. (C) Memristor conductance evolution with the applied pulse trains in (B). Each data point is averaged from 128 devices. (D) The average change in conductance (ΔG , left y axis) after applying different pulse trains, showing that ΔG increases with the input signal variations (right y axis).

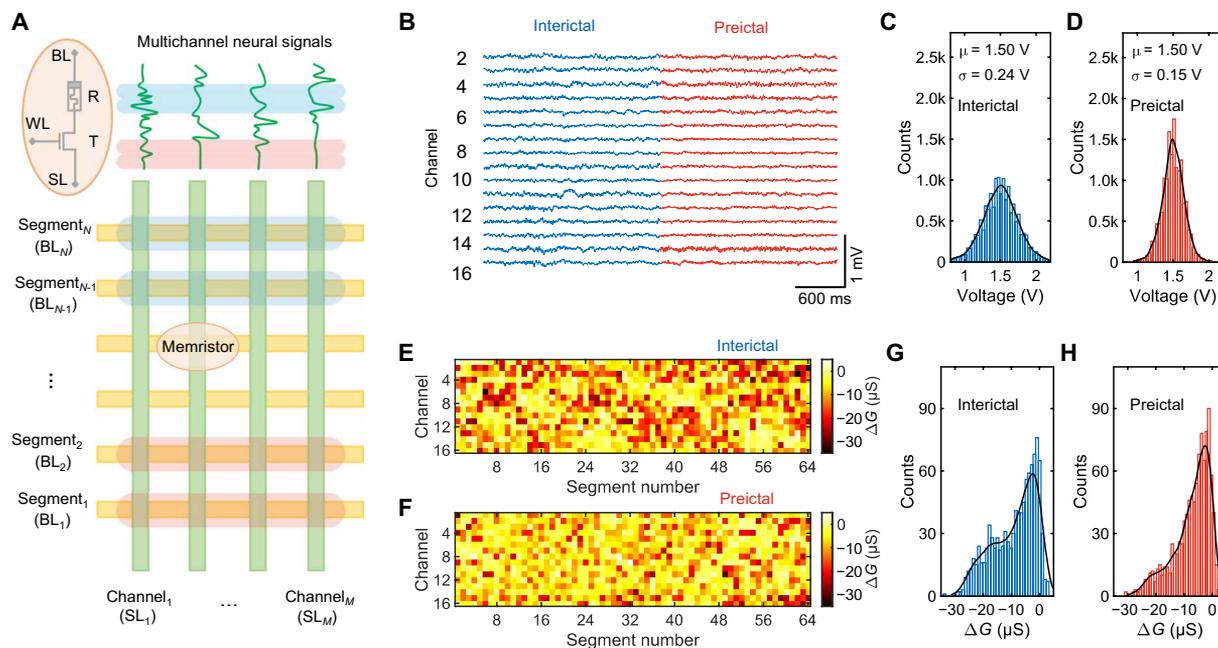


Fig. 3. Parallel multichannel processing of neural signals. (A) Illustration of the signal segment scheme in memristor array. (B) Waveforms of typical 16-channel interictal and preictal signal clips. Blue, interictal. Red, preictal. The sampling rate is 400 Hz. (C and D) Histograms of the input voltage after the linear transformation of raw interictal and preictal neural signals, respectively. Gain = 10^4 and $V_{\text{offset}} = 1.5$ V. (E and F) Conductance change map after processing the interictal and preictal signal clips in the memristor array, respectively. (G and H) Histograms of the conductance change (ΔG) in (E) and (F), respectively.

of recording channels, length, and sampling rate of the neural signals to be processed as well as the memristor operation conditions.

An example set of 16-channel preictal and interictal iEEG signals from the Kaggle Seizure Prediction Dataset (see Materials and Methods for the dataset details) is shown in Fig. 3 (B and C). For more recording channels and longer signal durations in practical applications, the memristor array size can be scaled up accordingly. The distributions of input voltages (linearly transformed from raw data with the same amplification gain of $\text{Gain} = 10^4$ and offset of $V_{\text{offset}} = 1.5 \text{ V}$) for the two sets of preictal and interictal signals are compared in Fig. 3 (C and D). Figure 3 (E and F) plots the ΔG maps after both signals are processed in the memristor array in parallel. The distributions of the output ΔG are shown in Fig. 3 (G and H). It is found that the interictal signals have a similar mean value ($\sim 1.5 \text{ V}$) but a much larger SD (0.24 V versus 0.15 V) than the preictal signals, resulting in more memristor devices having large conductance changes (e.g., $|\Delta G| > 15 \mu\text{S}$).

To further optimize the memristor array-based system for neural signal processing, a systematic study is carried out using different experiment conditions. For example, fig. S3 compares the system performance when using the input signals for SET and RESET operations. It is found that the RESET operation leads to a much larger contrast between the intra- and intersignal correlations, which is in part because that the RESET process is more gradual than SET, as can be seen from Fig. 2A and fig. S1B. We should mention that the system performance could also be affected by the characteristics of memristors (such as the on/off ratio, number of states, and linearity of conductance modulation; see discussions in fig. S3) and the linear

transformation conditions (e.g., offset and amplification gain) of neural signals. For example, fig. S4A shows the correlations as a function of the amplification gain in Eq. 1 ($V_{\text{offset}} = 1.5 \text{ V}$). In the range from 0.7×10^4 to 1.7×10^4 , the bigger the gain is, the larger the correlation contrast is, and, hence, the better the performance is. Similarly, fig. S4B shows the correlations as a function of V_{offset} ($\text{Gain} = 10^4$). In the range from 1.2 to 1.5 V, the smaller the offset is, the better the performance is. All these results indicate that there is a large optimization space to improve the system performance for practical applications. Future studies are needed to further investigate the effects of the memristor conductance modulation characteristics and neural signal linear transformation conditions on the system performance.

Robustness analysis

For practical applications, the robustness of the memristor array-based system for multichannel neural signal processing is further analyzed in both temporal and spatial scales. The robustness in time scale is verified by carrying out 200 trials where the first 100 trials use the same interictal signals, while the other 100 trials use the same preictal signals. All signals are processed in the same memristor array. Figure 4A shows the correlation map between the corresponding ΔG maps (see Materials and Methods for the calculation of correlation coefficient). The intersignal correlation is very low (< 0.2), while the intrasignal correlation is high (> 0.7). This result confirms that the processed neural signals in the memristor array retain sufficient information on the resulting ΔG that can be used to distinguish preictal and interictal signals. In practical applications,

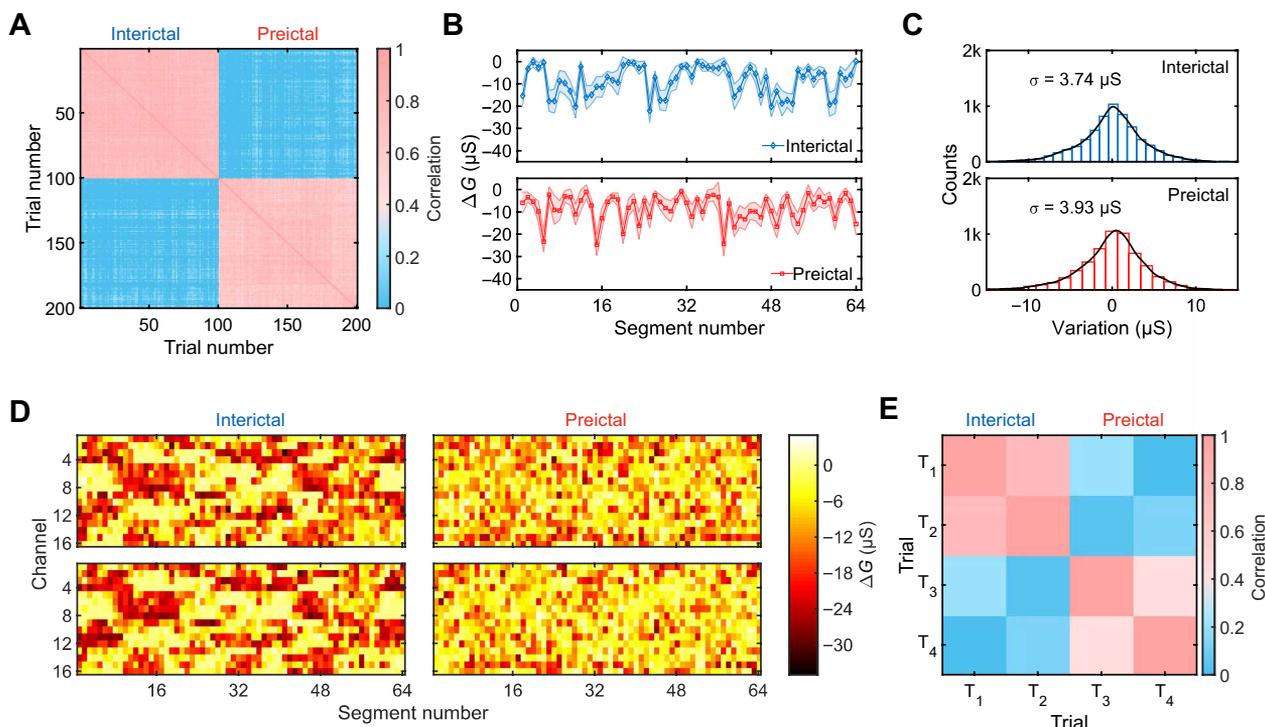


Fig. 4. Robustness analysis of the memristor array-based system for multichannel neural signal processing. (A) The correlation matrix of the output ΔG in different trials. Interictal and preictal signals are used in first 100 and last 100 trials, respectively. (B) Shaded error bar plot of ΔG waveforms for the corresponding signals. (C) Distributions of ΔG variation in both interictal and preictal trials. (D) ΔG maps for different trials where the same sets of interictal and preictal neural signals are applied to two different memristor arrays. Trails from up to bottom and from left to right are labeled as T_1 to T_4 accordingly. (E) Correlation matrix between different trials. T_1 and T_2 : The trials where the same interictal signal clip is applied to arrays #1 and #2, respectively. T_3 and T_4 : The trials where the same preictal signal clip is applied to arrays #1 and #2, respectively.

it is also important for the memristors to maintain their characteristics during repeated operations to process large-volume neural signal data from the brain. For this purpose, we investigate the endurance characteristics of our memristors, and the result shows that it can reach over 2×10^9 cycles (fig. S5). Our previous work also confirmed that the endurance for analog switching can be further extended up to $\sim 10^{11}$ cycles by adjusting the switching conductance range (41). We can then roughly estimate that our memristors could support continuous processing of neural signals for at least 5 years (see Materials and Methods for the estimation details). This lifetime is already sufficient for most typical applications, and it can be further extended by using a memristor array with larger number of columns.

It is noted that there are variations in the trial-to-trial experimental results, mainly due to the cycle-to-cycle variation in memristors (24). Figure 4B shows the trial-to-trial ΔG waveforms of processing results. Figure 4C plots the ΔG variations for interictal and preictal signals, showing similar distributions with small SD ($3.74 \mu\text{S}$ versus $3.93 \mu\text{S}$). Along with Fig. 4A, it is suggested that the trial-to-trial variation is quite small and, hence, does not prevent the system from distinguishing interictal and preictal signals. In addition, the device-to-device variation in the memristor array could also affect the system performance. To investigate this effect, we process the same clip of neural signals on the 16 channels in a memristor array, as shown in fig. S6. The results indicate that different channels in the memristor array show similar output ΔG patterns for the same input signals (fig. S6, E and F). To further verify the spatial-scale, i.e., array-level, robustness of memristors for multichannel processing of neural signals, two new

sets of 16-channel iEEGs are processed on two different memristor arrays, and the results are summarized in Fig. 4 (D and E). Again, the interictal and preictal signals can be distinguished, as evident from the correlation maps. Future device optimizations to reduce the variability of the memristor array are expected to further improve the system performance.

Seizure prediction using processed results

After the input signals are processed on the memristor array, the conductance (or equivalently ΔG changed from the same initial conductance) of all the memristor devices can be read out for further analysis, such as feature extraction and classification, which can be done by general machine learning algorithms. For proof-of-concept demonstration, here we can simply use the number of devices in specific ΔG ranges to demonstrate epileptic seizure prediction. The reason for using the number of devices in specific ΔG as the inputs for classification is that the processed results, i.e., ΔG distributions, are capable of representing the signal energy and variations, as shown above. As plotted in Fig. 5 (A and B), the distribution of ΔG from interictal signals is more dispersive than that from preictal signals, as can be measured by variations, although they have similar signal energies.

To demonstrate the feasibility of epileptic seizure prediction using the proposed approach, 60 sets of preictal and interictal iEEG signals are processed in our memristor array as described above. The numbers of devices with $\Delta G \in (-35 \mu\text{S}, -27 \mu\text{S})$ (F_1), $\Delta G \in (-16 \mu\text{S}, -9 \mu\text{S})$ (F_2), and $\Delta G \in (-7 \mu\text{S}, 0 \mu\text{S})$ (F_3) are used as the extracted features. A linear classifier is designed using the linear discriminant

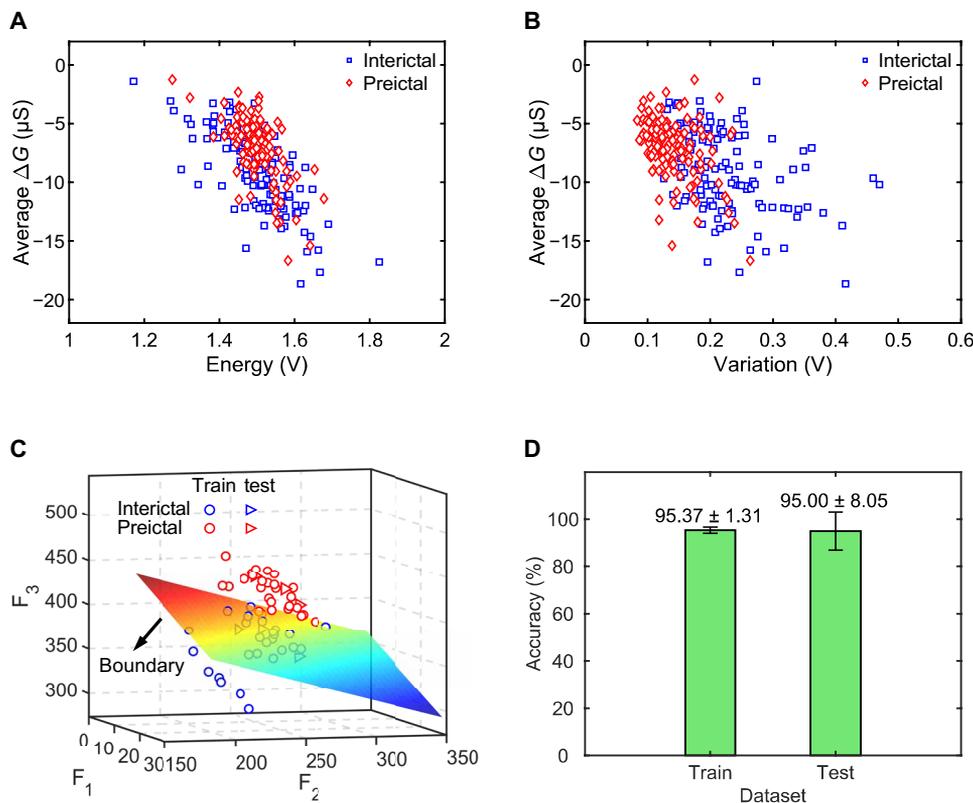


Fig. 5. Analysis of memristor-processed results for seizure prediction. (A) Average ΔG versus signal energy of eight consecutive segments. (B) Average ΔG versus signal variation of eight consecutive segments. (C) Training results of the LDA classifier for 54 clips of 16-channel signals plotted along with testing results of the trained LDA classifier for 6 clips of 16-channel signals. F_1 , F_2 , and F_3 represent the numbers of devices with ΔG in the specific ranges of $(-35 \mu\text{S}, -27 \mu\text{S})$, $(-16 \mu\text{S}, -9 \mu\text{S})$, and $(-7 \mu\text{S}, 0 \mu\text{S})$, respectively. (D) The training and testing accuracies from the 10-fold cross-validation.

analysis (LDA) (42) to classify the interictal and preictal signals. To be fair, we use 10-fold cross-validations to train and test the classifier. Figure 5C shows the results for 1 of 10 trials. The average accuracies of the 10 training and testing trials are 95.33 and 95.00%, respectively (Fig. 5D), which are remarkable using a simple linear classifier that can be conveniently implemented in hardware. The average sensitivity and specificity for all testing trails are 93.33 and 96.67%, respectively (see Materials and Methods for the detailed calculations). It should be noted that more features can be extracted from the processed results of multichannel neural signals to handle more complex datasets and achieve higher classification accuracy.

DISCUSSION

Last, the memristor-based hardware system performance is compared with related literature work using memristor and also benchmarked against complementary metal-oxide semiconductor (CMOS) application-specific integrated circuit (ASIC) chips designed for neural signal processing. The comparison is detailed in Materials and Methods for the task of processing one clip of 16-channel neural signals with a sampling rate of 10 kHz (~1-s duration). The power efficiency of 60.81 nW per channel in this work shows roughly three-orders-of-magnitude improvements compared with literature-reported ~80 μ W per channel for CMOS ASICs. Therefore, our system shows substantial advantages in parallel processing of multichannel neural signals with low power.

In addition to the power advantage and high scalability, our memristor array-based system also has the potential of real-time processing by using two memristor arrays to work alternatively for the conductance modulation and reading steps. Also, in our approach, the input signals are segmented and applied directly to the corresponding memristors, which inherently eliminates the need for data buffers for temporarily storing neural signal clips. In addition, our system carries out intensive computation and compresses the results into device conductance, reducing the need of complex circuit modules for computations and extra storages for intermediate and final data. These advantages could help markedly reduce the chip area, which is also a critical challenge for implanted biomedical electronics.

In conclusion, we have designed a highly scalable low-power hardware system for parallel processing of multichannel neural signals based on memristor arrays. Furthermore, epileptic seizure prediction with high accuracy over 95% has been demonstrated on the basis of the experimentally processed results to verify the feasibility and efficiency of the system. The analog conductance modulation behaviors of our memristors allow us to extract the critical amplitude and variation information of input signals and encode in the memristor conductance change. With the developed signal segmentation scheme in the memristor array, the system has shown excellent robustness against device variabilities. Our work highlights the great potential of using memristor arrays for massively parallel processing multichannel neural signals with high fidelity and power efficiency, which are critical for future fully implantable neural interfaces.

MATERIALS AND METHODS

Memristor fabrication

In the 1T1R structure, a transistor serves as the selector, and the resistive switching layers are fabricated on the top of the transistor's

drain terminal. For our 1k-cell memristor array, the transistor array is fabricated in a commercial foundry with 0.13- μ m CMOS process. The remaining process steps are completed in the laboratory. For more details about the device fabrication, please see our previous works (23, 43).

Programming and reading schemes of the memristor-based system

We illustrate our detailed system overview in fig. S1. In this figure, we present an $m \times n$ memristor array with peripheral circuits, where m and n represent the number of channels and segments, respectively. This design supports four operation modes including FORM, SET, PROCESS, and READ. The first three modes are used to electroform, set, and reset the memristors, respectively. The PROCESS mode is chosen to parallel process multichannel neural signals through RESET operations in this work. In the READ mode, 3-bit-resolution current sensing amplifier (CSA) serves as the readout circuit. Figure S7 illustrates the programming scheme in the PROCESS mode. The activated BL and modules to process a certain segment of neural signals are color labeled, while those unused ones are drawn in gray. The parallelism is achieved in this mode by applying multichannel input signals to memristors in one column (i.e., segment) to modulate their conductances at the same time. The shift register controls and chooses to which memristor column the input signals are applied, and every time, there is only a WL turned on. Similarly, fig. S8 shows the read scheme of the memristor array in the READ mode. When sensing and digitalizing the currents, CSAs clamp the SL voltages to 0.15 V, which is the read voltage, and then compare the currents with reference currents. Figure S9 presents the FORM and SET schemes for the array. In these two modes, the memristor could be programmed in parallel or sequential fashion.

Multichannel neural signal dataset

The 16-channel neural signals are from the widely used open-access dataset, Kaggle Seizure Prediction Dataset (www.kaggle.com/c/seizure-prediction/). This dataset includes multichannel neural signals from four dogs and two human patients. In our work, the neural signals sampled at 400 Hz from "dog 2" are used. We randomly select 60 sets of interictal and preictal signals for classification. Here, the preictal signals refer to the brain signal clips recorded tens of minutes before the epileptic seizure onset, and the interictal signals are recorded from the brain at least 1 week before the next seizure occurs.

Correlation coefficient and its calculation

The correlation coefficient, denoted by r , is a statistic for measuring the linear relationship between two sets of data. The value of r is between -1 and 1 . The closer its absolute value is to 1 , the better these two datasets can be expressed by a linear equation. There are little or no linear relations between them if r is close to 0 . For any given two vectors \mathbf{x} , \mathbf{y} with the same length N , their correlation coefficient r can be calculated using the following equation

$$r = \frac{\sum_1^N (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum_1^N (x_i - \bar{x})^2 (y_i - \bar{y})^2}} \quad (2)$$

where \bar{x} and \bar{y} are the mean values of \mathbf{x} and \mathbf{y} , respectively.

Estimation of the lifetime of the memristor array

Figure S5 shows that the typical endurance of our memristors can reach over 2×10^9 cycles. With such a long endurance of memristor, we do not observe any apparent degradation on the system accuracy in our experiments. In this work, we use neural signals sampled at 400 Hz as the input for our memristor array, so each device is subjected to 15 RESET voltage pulses (i.e., one segment) in processing one clip (64 segments) of neural signals with a length of 2.4 s. We can then roughly estimate that such an endurance of 2×10^9 cycles could continuously process neural signals with a duration of $2 \times 10^9 / 30 \times 2.4 \text{ s} = 1.6 \times 10^8 \text{ s} > 5$ years, assuming that the same number of SET pulses (15) is needed to initialize the memristor conductance after each segment. Therefore, the lifetime of our memristor array is sufficient for most applications.

Performance evaluation of epileptic seizure prediction

In the prediction, the preictal samples are regarded as the positive samples, while the interictal samples are the negative samples. The results from the LDA classifier can be divided into four categories: true positive, false negative, true negative, and false negative. Here “true” and “false” represent the correct and incorrect predictions, respectively. To evaluate the prediction performance, three statistical metrics, including accuracy, sensitivity, and specificity, are calculated as follows

$$\text{Accuracy} = \frac{\text{TP} + \text{TN}}{\text{TP} + \text{TN} + \text{FP} + \text{FN}} \quad (3)$$

$$\text{Sensitivity} = \frac{\text{TP}}{\text{TP} + \text{FN}} \quad (4)$$

$$\text{Specificity} = \frac{\text{TN}}{\text{TN} + \text{FP}} \quad (5)$$

Power efficiency estimation and comparison

For the estimation of power efficiency, we use a task of processing 16-channel neural signals that are sampled at 10 kHz. The whole task can be divided into two parts: multichannel signal processing and then reading of the memristor conductance states. To compare with CMOS ASICs, each memristor is applied 16 consecutive input pulses, similar to the 15-pulse experiment in our demonstration. Then, a clip of signals with 10,240 samples in each channel could be processed in a 16×640 memristor array for estimating the power efficiency.

Modules used for the multichannel signal processing step are shown in fig. S7. To process the task defined above, the energy consumed in the array operations can be calculated as $(2 \text{ V})^2 \times 30 \mu\text{S} \times 50 \text{ ns/pulse} \times 16 \times 640 \times 16 = 983.04 \text{ nJ}$, where 2 V is the upper bond of the input voltage amplitude since the input voltage pulses are linearly transformed to the range of 1 to 2 V, as shown in Fig. 3 (C and D). Here, $30 \mu\text{S}$ is the initial memristor conductance, and 50 ns is the pulse width. The energy consumed by peripheral circuits are calculated as follows: $0.6 \mu\text{W} \times 50 \text{ ns/pulse} \times 16 \times 16 \text{ pulse} \times 640 = 4.92 \text{ nJ}$ for the 640 BL multiplexers (MUXs) and $0.6 \mu\text{W} \times 50 \text{ ns/pulse} \times 16 \times 16 \text{ pulse} \times 640 = 4.92 \text{ nJ}$ for the 16 SL MUXs, where $0.6 \mu\text{W}$ is the power consumption of a BL/SL MUX in the PROCESS mode. In the programming scheme of the PROCESS mode, the shift register only has negligible dynamic power consumption, which is estimated as $10 \text{ kHz}/16 \times (5 \text{ V})^2 \times 10 \text{ fF} \times (10,240 \text{ samples}/10 \text{ kHz}) = 0.16 \text{ nJ}$, where 5 V represents the source voltage and 10 fF is the transistor gate capacitor. Thus, the total energy is estimated as 993.04 nJ for this step.

Modules used for the READ mode are shown in fig. S8. During the above task, the energy consumed in the memristor devices can be estimated as $(0.15 \text{ V})^2 \times 30 \mu\text{S} \times 50 \text{ ns/pulse} \times 16 \times 640 \times 16 = 0.35 \text{ nJ}$, where 0.15 V is the read voltage. The energy consumed by peripheral circuits are calculated as follows: $0.045 \mu\text{W} \times 50 \text{ ns/pulse} \times 16 \text{ pulse} \times 640 \times 16 = 0.37 \text{ nJ}$ for the 640 BL MUXs and $0.045 \mu\text{W} \times 50 \text{ ns/pulse} \times 16 \text{ pulse} \times 640 \times 16 = 0.37 \text{ nJ}$ for the 16 SL MUXs, where $0.045 \mu\text{W}$ is the power consumption of a BL/SL MUX in the READ mode. The 16 CSAs consume $4 \mu\text{W} \times 50 \text{ ns} \times 16 \times 640 = 2.05 \text{ nJ}$ energy to sense and digitize the output conductances, where $4 \mu\text{W}$ is estimated through simulation for the power consumption of an CSA. Similarly, the shift register has a small dynamic power consumption of 0.16 nJ. Thus, the total energy is 3.30 nJ for this step.

To calculate the power efficiency, we first estimate the total energy consumption to be 996.34 nJ. Hence, the power efficiency is estimated as $996.34 \text{ nJ}/(10,240 \text{ samples}/10 \text{ kHz})/16 \text{ channel} = 60.81 \text{ nW}$ per channel. For CMOS-based counterparts, (2) reported an ASIC chip for epileptic seizure control, in which the biosignal processing unit consumes 2.5 mW in total to carry out feature extraction based on 128-point fast Fourier transformation and entropy computation for classification based on 16-input ridge regression model. Thus, its power efficiency is calculated as $2.5 \text{ mW}/16 \text{ channel} = 156.2 \mu\text{W}$ per channel. Cheng *et al.* (44) reported another ASIC chip that has a similar power efficiency of 163.2 μW per channel. It is estimated that over 50% power is consumed by feature extraction for these two ASIC chips based on the amount of computations for feature extraction and classification. Therefore, the memristor-based neural signal processing system shows more than 1000 \times advantage in power efficiency than its CMOS-based counterparts (60.81 nW per channel versus $\sim 80 \mu\text{W}$ per channel).

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at <http://advances.sciencemag.org/cgi/content/full/6/41/eabc4797/DC1>

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