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Supplementary Materials for

Moisture-triggered physically transient electronics

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Synthesis scheme of the humidity-controlled degradable polymer

1. Clean a 5 ml vial (acetone, isopropyl alcohol (IPA), deinoized (DI) water).
2. Dry the vial at 100 ^{o}C for 10 min.
3. Add 4-pentenoic anhydride (131.2 mg; 0.72 mmol), poly(ethylene glycol) diacrylate (20 mg; 0.08 mmol), pentaerythritol tetrakis(mercaptoacetate) (173 mg; 0.4 mmol), and 2,2-Dimethoxy-2-phenylacetophenone (3 mg, 0.012 mmol) sequentially into the vial.
4. Mix and dissolve all the components through vortex mixing and ultrasonication.
5. Prepare a mold with two glass slides separated by two pieces of cover glass.
6. Inject the mixture into the mold through a syringe.
7. Solidify the mixture through a UV curing lamp (BOEKEL SCIENTIFIC Inc. Model: 234100) for 3 min.
8. Peel off the cured polymer film using a blade.

Preparation scheme of shadow masks

1. Spin-coat (1000 rpm for 30s) a thin layer of PDMS (1 : 10) on a cleaned glass and cure to form an adhesive layer.
2. Laminate polyimide (PI) film (25.4 μm Kapton film, Dupont) onto the PDMS surface.
3. Clean the PI film (acetone, IPA, DI water).
4. Dry the PI on hotplate at 90^{o}C for 10min.
5. Deposit 500 nm copper (Cu) as the etching mask onto the PI using e-beam evaporation.
6. Spin-coat photoresist (PR; Clariant AZ5214, 2000 rpm, 30 s) and soft-bake at 110 ^{o}C for 1 min.
7. Expose with 365 nm UV at a dose of 150mJ/cm^{2}.
8. Post-bake at 120 ^{o}C for 2 min.
9. Expose with 365 nm UV at a dose of 200mJ/cm^{2}.
10. Develop in aqueous base developer (Clariant AZ917 MIF).
11. Etch the exposed Cu by Cu etchant (CE-100, Transene Co. Inc.).
12. Clean the PI film (acetone, IPA, DI water).
13. Etch the PI using reactive ion etching (oxygen: 40 sccm, power: 250 W) for 8 hours.
14. Peel off the PI film from the PDMS surface.
15. Etch the Cu on PI by Cu etchant.

16. Clean the PI film (acetone, IPA, DI water).

Preparation scheme of the metal and oxide membranes onto the polymer

1. Prepare a PI based shadow mask with dot array.
2. Laminate the shadow mask onto a polymer substrate.
3. Deposit metal and oxide dots onto the polymer using e-beam evaporation or sputtering.

Fabrication of the Cu resistor and antenna onto the polymer

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the Cu onto the polymer using e-beam evaporation.
3. Peel the shadow mask off from the polymer.

Fabrication of the capacitor onto the polymer

Bottom electrode deposition

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the Cu onto the polymer using e-beam evaporation.
3. Peel the shadow mask off from the polymer.

Dielectric layer deposition

4. Align and laminate the shadow mask onto a polymer substrate.
5. Deposit the MgO onto the polymer using e-beam evaporation.
6. Peel the shadow mask off from the polymer.

Top electrode deposition

7. Align and laminate the shadow mask onto a polymer substrate.
8. Deposit the Cu onto the polymer using e-beam evaporation.
9. Peel the shadow mask off from the polymer.

Fabrication of the field-effect transistor and inverter onto the polymer

Indium-gallium-zinc-oxide (IGZO) deposition

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the IGZO onto the polymer by DC sputtering under 20W and 4% of oxygen partial pressure to argon using $InGaZnO_4$ target

3. Peel the shadow mask off from the polymer.

Source and drain electrode formation

4. Align and laminate the shadow mask onto a polymer substrate.
5. Deposit the Cu onto the polymer using e-beam evaporation.
6. Peel the shadow mask off from the polymer.

Gate dielectric deposition

7. Align and laminate the shadow mask onto a polymer substrate.
8. Deposit the MgO onto the polymer using e-beam evaporation.
9. Peel the shadow mask off from the polymer.

Gate electrode formation

10. Align and laminate the shadow mask onto a polymer substrate.
11. Deposit the Cu onto the polymer using e-beam evaporation.
12. Peel the shadow mask off from the polymer.

Fabrication of the Schottky diode onto the polymer

Indium-gallium-zinc-oxide (IGZO) deposition

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the IGZO onto the polymer by DC sputtering under 20W and 4% of oxygen partial pressure to argon using $InGaZnO_4$ target
3. Peel the shadow mask off from the polymer.

Schottky contact formation

4. Align and laminate the shadow mask onto a polymer substrate.
5. Deposit the Ni onto the polymer using e-beam evaporation.
6. Peel the shadow mask off from the polymer.

Ohmic contact formation

7. Align and laminate the shadow mask onto a polymer substrate.
8. Deposit the Al onto the polymer using e-beam evaporation.
9. Peel the shadow mask off from the polymer.

Fabrication of the UV detector onto the polymer

Indium-gallium-zinc-oxide (IGZO) deposition

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the IGZO onto the polymer by DC sputtering under 20W and 4% of oxygen partial pressure to argon using $InGaZnO_4$ target
3. Peel the shadow mask off from the polymer.

Electrode formation

4. Align and laminate the shadow mask onto a polymer substrate.
5. Deposit the Cu onto the polymer using e-beam evaporation.
6. Peel the shadow mask off from the polymer.

Fabrication of the resistive memory onto the polymer

Bottom electrode metallization

1. Laminate the shadow mask onto a polymer substrate.
2. Deposit the Cu onto the polymer using e-beam evaporation.
3. Peel the shadow mask off from the polymer.

Indium-gallium-zinc-oxide (IGZO) deposition

4. Align and laminate the shadow mask onto a polymer substrate.
5. Deposit the IGZO onto the polymer by DC sputtering under 20W and 4% of oxygen partial pressure to argon using $InGaZnO_4$ target
6. Peel the shadow mask off from the polymer.

Top electrode metallization

7. Align and laminate the shadow mask onto a polymer substrate.
8. Deposit the Cu onto the polymer using e-beam evaporation.
9. Peel the shadow mask off from the polymer.

Tuning of components in the polymer preparation

Through the manipulation of the poly(pentenoic anhydride) components, the hydrolysis behavior of the polymer can be controlled. We have prepared the polymer with different amount of poly(pentenoic anhydride) according to table S1.

table S1. Precursors for polyanhydride films with different compositions (the calculation depends on the PEG molar ratio in the mixture).

PGE ratio (%)	4-Pentenoic anhydride mg (mmol)	PEG mg (mmol)	PentaerythritolTetrakis (mercaptoacetate) mg (mmol)	DMPA mg (mmol)
0	145.8 (0.80)	0(0)	173(0.4)	3 (0.012)
10	131.2 (0.72)	20 (0.08)	173(0.4)	3 (0.012)
20	116.6 (0.64)	40 (0.16)	173(0.4)	3 (0.012)
30	102.0 (0.56)	60 (0.24)	173(0.4)	3 (0.012)
40	87.5 (0.48)	80 (0.32)	173(0.4)	3 (0.012)
50	72.9 (0.40)	100 (0.40)	173(0.4)	3 (0.012)

Characterization of the resistor

The resistances over time were measured by KEITHLEY 4200-SCS during device dissolving.

Characterization of the antenna

The antenna was placed on a copper ground and fixed by an SMA probe. The Cu antenna was characterized by National Instrument PXIe-5630 vector network analyzer during device dissolving.

Characterization of the capacitor

The capacitance of metal-insulator-metal structured capacitor based on MgO was directly measured by an LCR meter (BK PRECISION 889) which was connected to a probe station. The measured capacitances of the devices were biased at 250mV at the frequencies of 100Hz, 120Hz, 1kHz, 10kHz, and 100kHz.

Characterization of the TFT

The TFTs was characterized by KEITHLEY 4200-SCS. The output curve of the device was measured with the V_{ds} swept from 0V to 20V at stepped V_{gs} (from 0V to 20V with a step of 2V).

The transfer curve was measured by sweeping V_{gs} from -10V to 20V at constant V_{ds} of 20V. The field effect mobility was extracted from the plot of the $I_{ds}^{1/2}$ versus V_{gs} using the following equation

$$I_{ds} = \left(\frac{WC_i}{2L}\right)\mu_{FE}(V_{gs} - V_{th})^2 \quad \text{(S1)}$$

where L, W, and Ci are the channel length, the width, and the gate capacitance per unit area, correspondingly. The threshold voltage (V_{th}) is defined as the voltage where the linear region of the $I_{ds}^{1/2}$ curve extend and intercept with the V_{gs}.

Characterization of the inverter

The voltage transfer curve was measured by KEITHLEY 4200-SCS. The V_{DD} was biased at 20V, and the V_{in} was swept from -5V to 30V, which is defined as logic 0 and logic 1. At low V_{in} state (logic 0), driver transistor is OFF state, then V_{out} will connect with V_{DD} (logic 1) since load transistor is ON. At high V_{in} state (logic 1), the driver transistor is ON state and the V_{out} connects to the ground to show logic 0. Gain versus V_{in} curve was obtained based on the following equation

$$\text{Gain} = -\frac{\partial V_{out}}{\partial V_{in}} \quad \text{(S2)}$$

Characterization of the Schottky diode

The diodes were characterized by KEITHLEY 4200-SCS.

Characterization of the photodetector

The devices were characterized under UV illumination and dark conditions using KEITHLEY 4200-SCS. UV75 Light THORLABS was used for UV light source that has the wavelength range from 300nm to 425nm and 40mW/cm^2 of intensity. The calculated average bright to dark current ratio was obtained by following equation

$$R = I_{bright}/I_{dark} \quad \text{(S3)}$$

Characterization of the resistive memory device

The resistive memory devices were characterized by KEITHLEY 4200-SCS. The retention test for low-resistance state (LRS) was carried out as the following: 1) setting by applying 10V; 2)

reading by applying constant voltage at 1V for 1000s; 3) resetting by applying -10V for high-resistance state (HRS); and 4) reading by applying constant voltage at 1V for 1000s. The write-read-erase-read cycle was characterized by applying the bias at 10V, 1V, -10V, and 1V correspondingly, in a repeating manner.

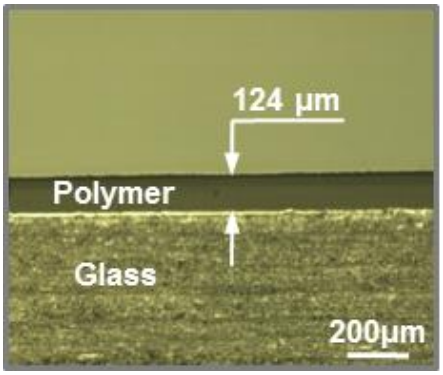

fig. S1. An optical image of the cross section of the polyanhydride substrate. The thickness of the polymer substrate is ~124 µm.

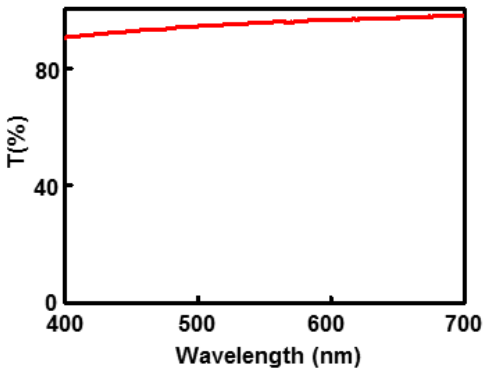

fig. S2. The transmittance spectrum of a moisture-sensitive polyanhydride thin film in visible range.

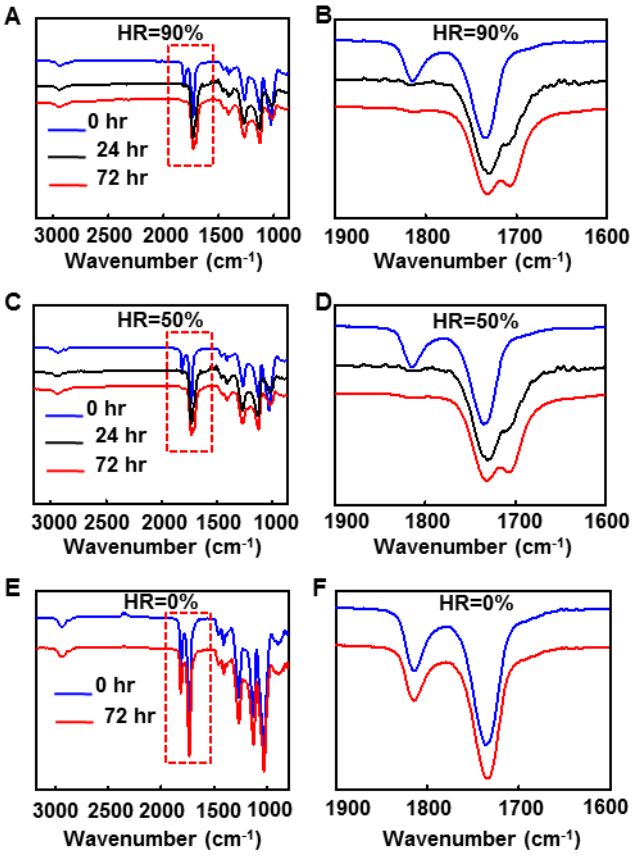

fig. S3. The time-sequential measurements of the FTIR spectra of the polymer thin films during the hydrolysis process under different relative humidity levels. (**A** and **B**) 90%, (**C** and **D**) 50%, and (**E** and **F**) 0%.

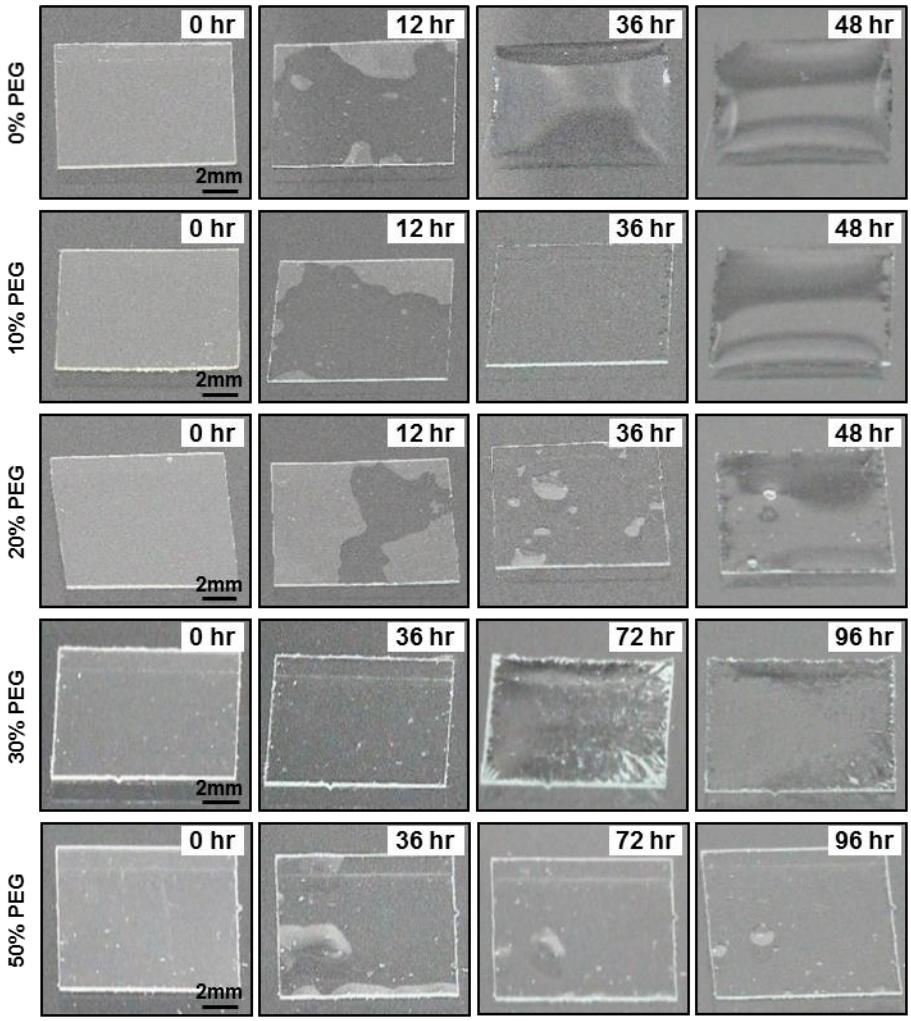

fig. S4. Optical images showing the time-sequential hydrolysis of the polymer with different compositions of PEG from 0 to 50% at a relative humidity of 90%.

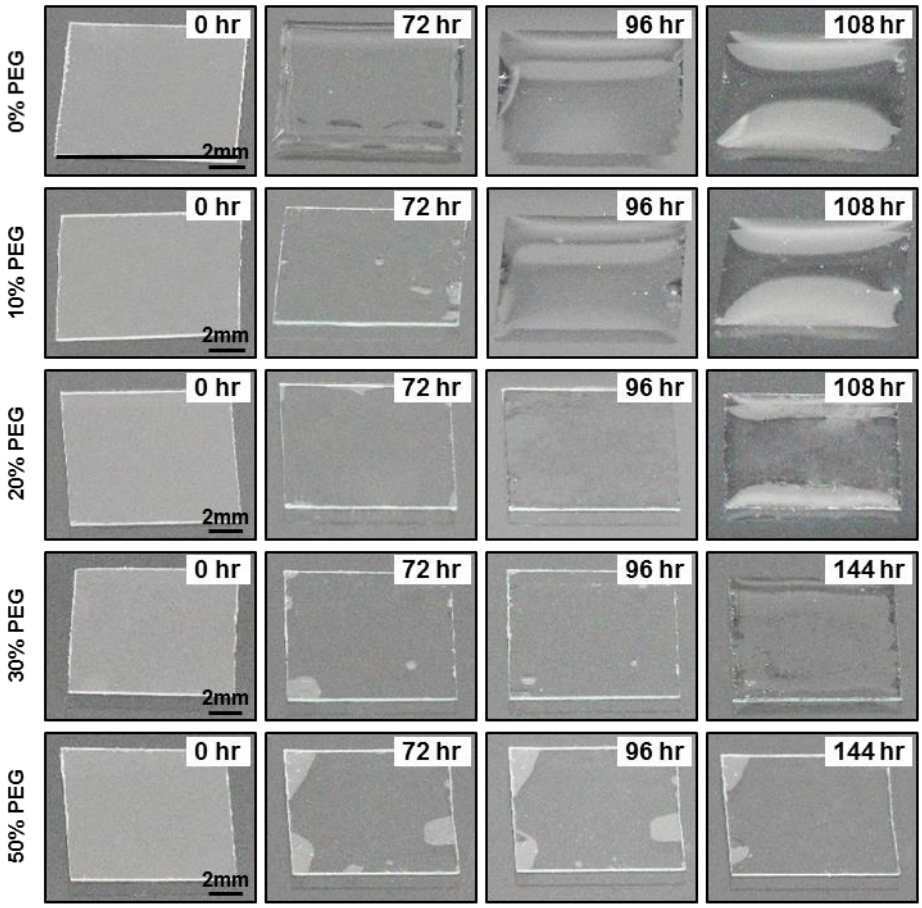

fig. S5. Optical images showing the time-sequential hydrolysis of the polymer with different compositions of PEG from 0 to 50% at a relative humidity of 45%.

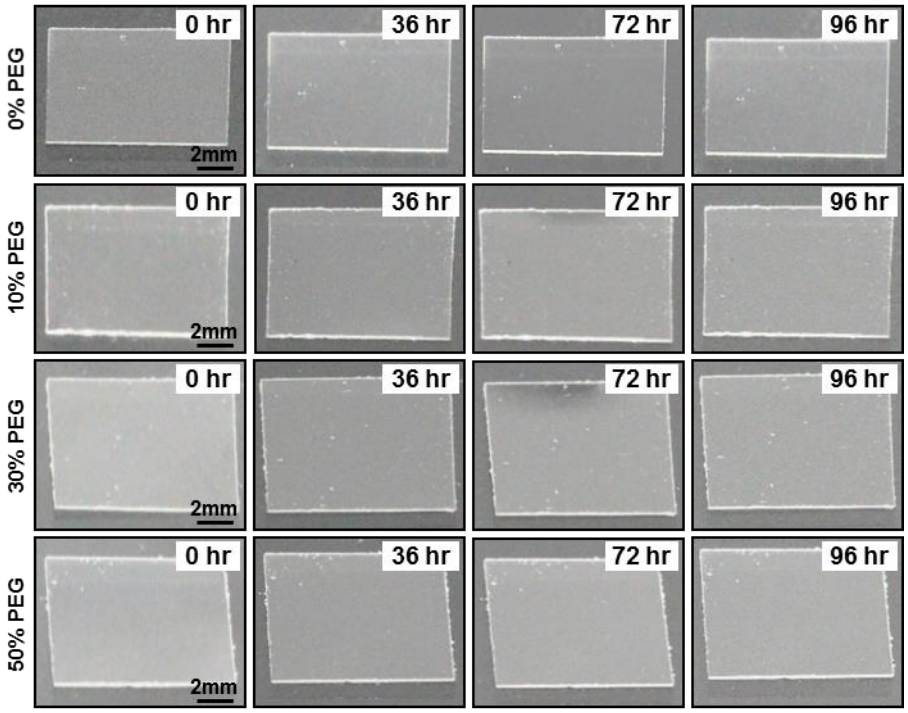

fig. S6. Optical images showing the time-sequential hydrolysis of the polymer with different compositions of PEG from 0 to 50% at a relative humidity of 0%.

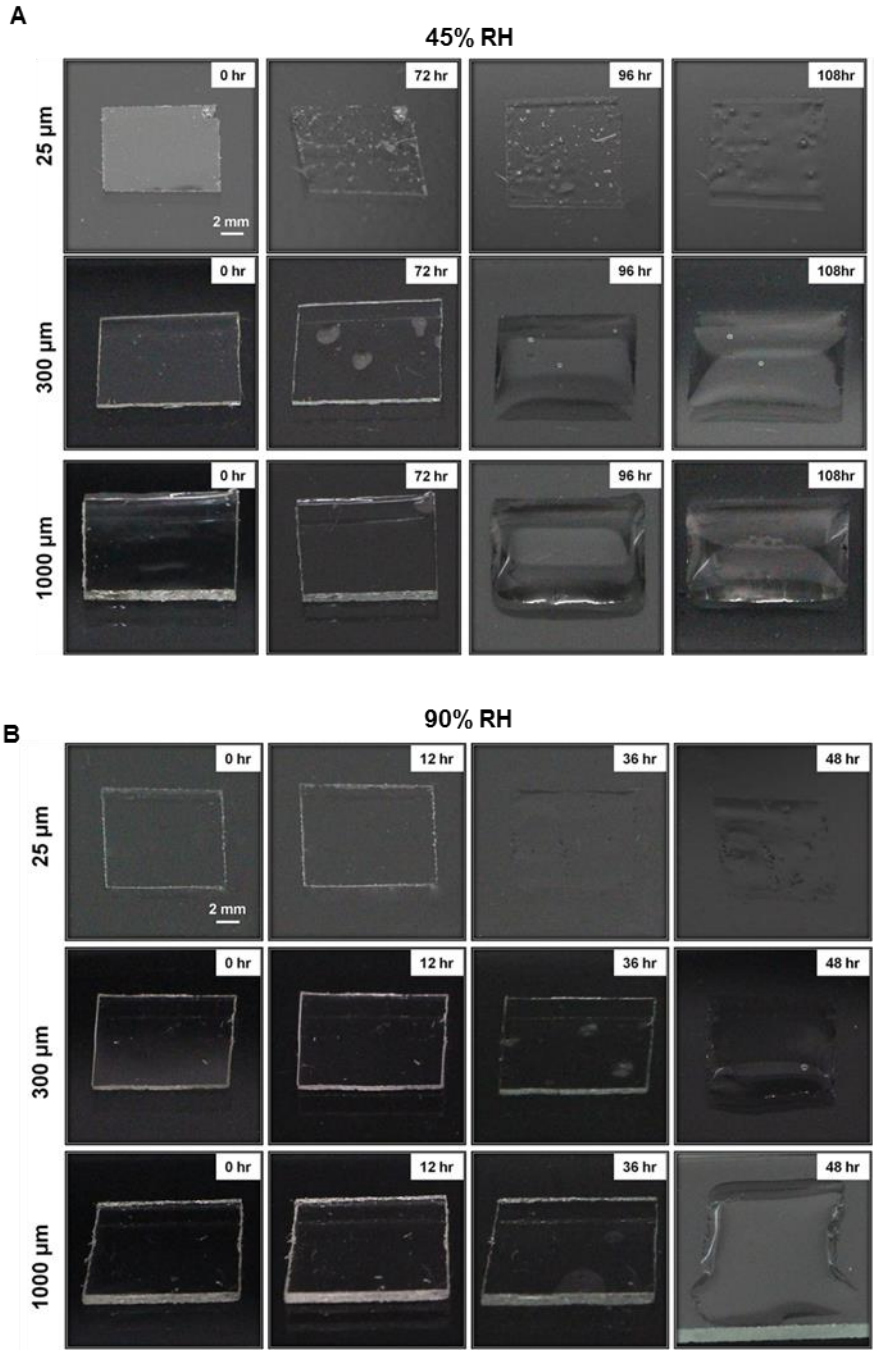

fig. S7. Optical images showing the time-sequential hydrolysis of the polymer substrates with different film thicknesses under different relative humidity levels. (**A**) 45%RH and (**B**) 90%RH. The polymer composition was identical for all polymer films (containing 10% PEG).

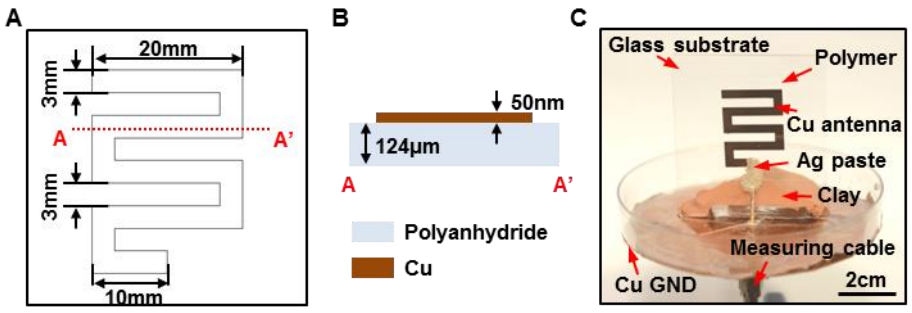

fig. S8. Cu antenna. (**A**) The planar and (**B**) cross-sectional dimensions of the Cu antenna. (**C**) The measurement setup.

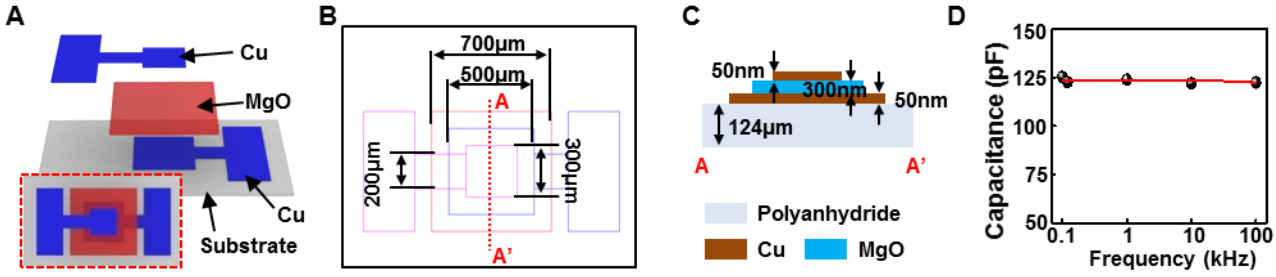

fig. S9. MgO-based capacitor. (**A**) A schematic illustration of the structure of the MgO based capacitor. The inset at the lower left is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the capacitor. (**D**) The measured capacitance before the transience starts.

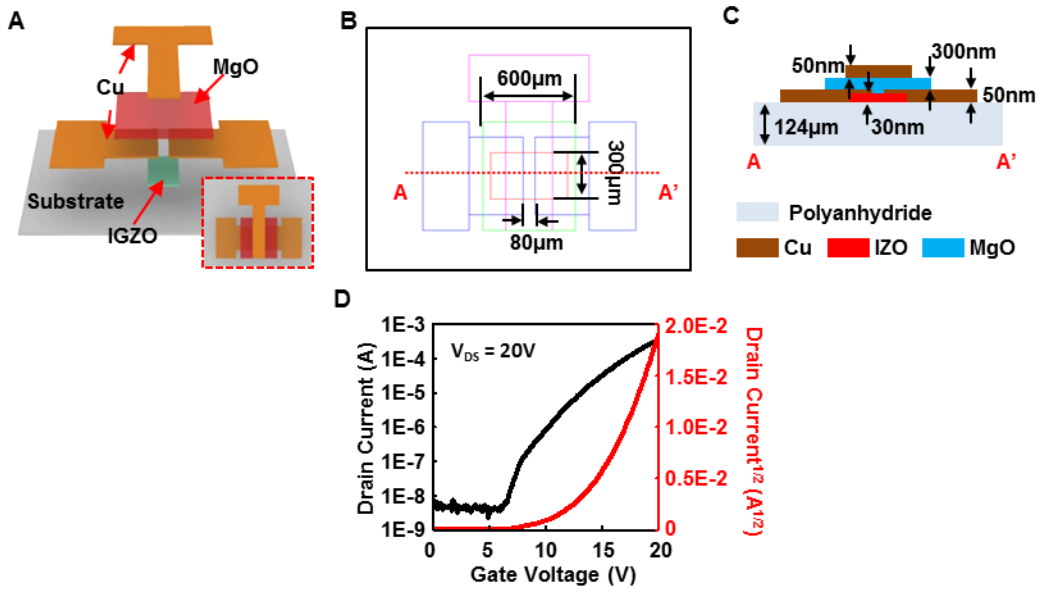

fig. S10. IGZO-based TFT. (**A**) A schematic illustration of the IGZO based TFT. The inset at the lower right is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the TFT. (**D**) Transfer characteristics of the TFT.

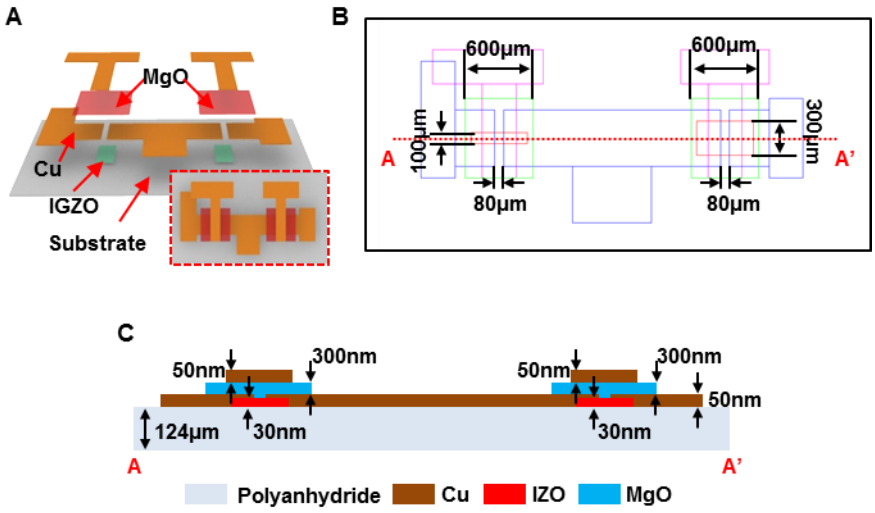

fig. S11. Logic gate inverter. (**A**) A schematic illustration of the logic gate inverter. The inset at the lower right of the figure is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the logic gate.

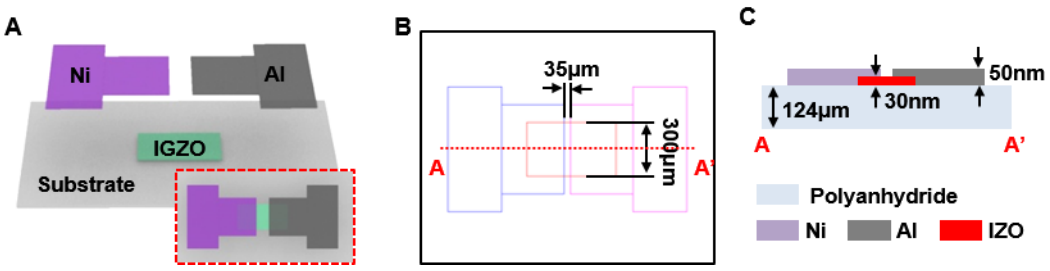

fig. S12. IGZO-based diode. (**A**) A schematic illustration the IGZO based diode. The inset at the lower right of the figure is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the diode.

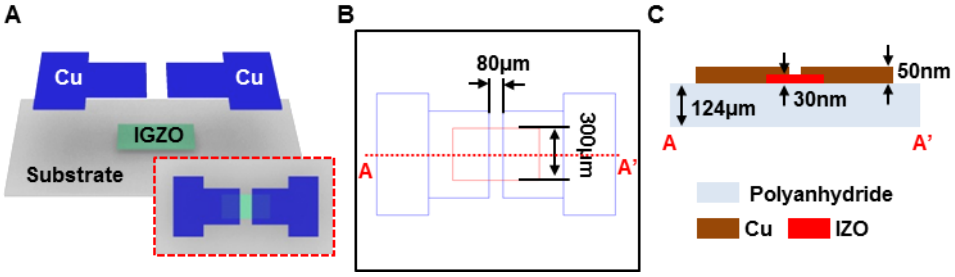

fig. S13. IGZO-based photodetector. (**A**) A schematic illustration of the IGZO based photodetector. The inset at the lower right of the figure is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the photodetector.

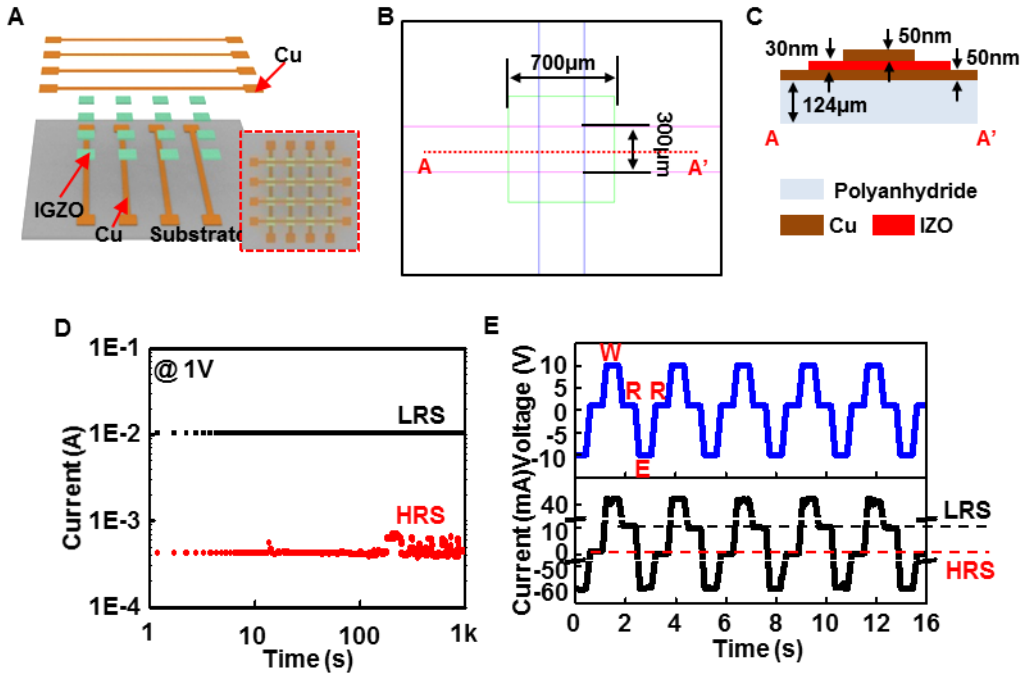

fig. S14. IGZO-based resistive memory. (**A**) A schematic illustration of the IGZO based resistive memory. The inset at the lower right of the figure is the top view of the device. (**B**) The planar and (**C**) cross-sectional layouts and dimensions of the device. (**D**) The retention test result and (**E**) WRER cycle result of the memory.